cPCI-9116

64-ch, 16-bit, 250KS/s Analog Input Card for
3U CompactPCI

User's Manual

Manual Rev.:	1.2
Revision Date:	July 7, 2020
Part No:	50-15002-1020

Leading **EDGE COMPUTING**

Revision History

Revision	Release Date	Description of Change(s)
1.10	2003-04-28	Initial release
1.2	2020-07-07	Update to current specification and software support.

Preface

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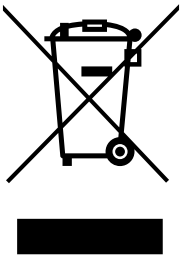

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Battery Labels (for products with battery)

California Proposition 65 Warning

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Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The cPCI-9116 series products are advanced data acquisition cards based on the 32-bit CompactPCI architecture. The cPCI-9116 series includes:

- cPCI-9116: 16-bit 250KHz DAS card for 3U CompactPCI

The cPCI-9116 series DAS cards use state-of-the-art technology making them ideal for data logging and signal analysis applications in the medical and process control industries.

1.1 Features

- 32-bit PCI bus, plug and play
- Up to 64 single-ended inputs or 32 differential inputs, mixing SE and DI analog signal sources
- 16-bit analog input resolution
- Onboard A/D 1K FIFO memory
- 512-word analog input channel gain queue spaces
- Sampling rate up to 250KS/s
- Bipolar or unipolar input signals
- Programmable gain of x1, x2, x4, x8
- Jumper-less and software configurable
- Five A/D trigger modes: software trigger, pre-trigger, post-trigger, middle-trigger and delay-trigger
- Software polling, interrupt and bus-mastering DMA data transfer available
- 8 digital input and 8 digital output channels
- 100-pin D-type SCSI-II connector
- Compact size: standard compact PCI 3U size

1.2 Applications

- Automotive testing
- Cable testing
- Transient signal measurement
- ATE
- Laboratory automation
- Biotech measurement

1.3 Specifications

1.3.1 Analog Input

- Converter: LT1606 (or equivalent) 250KHz
- Number of channels: (programmable)
  - 64 single-ended (SE)
  - 32 differential input (DI)
  - Mixing of SE and DI analog signal between channels allowed
- A/D Data FIFO buffer size: 1024 locations
- Channel gain queue length: 512-word configurations
- Resolution: 16-bit
- Input range: (controlled by channel gain queue)
  - Bipolar: ±5V, ±2.5V, ±1.25V, ±0.625V
  - Unipolar: 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25
- CMRR (DC to 60 Hz, typical)

Input Range	CMRR
±5, 0 to 10V	87dB
±2.5, 0 to 5V	90dB
±1.25, 0 to 2.5V	92dB
±0.625, 0 to 1.25V	93dB

- Overvoltage Protection: Continuous ±35V maximum

- Accuracy

Input Range	Accuracy
±5, 0 to 10V	0.01% of FSR
±2.5, 0 to 5V	0.02% of FSR
±1.25, 0 to 2.5V	0.02% of FSR
±0.625, 0 to 1.25V	0.04% of FSR

- Input Impedance: 100 MΩ | 6pF
- Time-base Source:
  - Internal 24MHz
  - External clock Input (fmax: 24MHz, fmin: 1MHz)
- Programmable scan interval and sampling rate (divided from time-base source)
- Trigger Mode:
  - Software-trigger
  - Pre-trigger
  - Post-trigger
  - Middle-trigger
  - Delay-trigger
- Data Transfer:
  - Polling
  - EOC interrupt transfer
  - FIFO half-full Interrupt transfer
  - Bus-mastering DMA
- Data Throughput: 250KHz (maximum)

1.3.2 Digital I/O (DIO)

- Channels: 8 TTL compatible digital inputs and outputs
- Input Voltage:
  - Low: VIL = 0.8 V max. IIL = 0.2mA max.
  - High: VIH = 2.0V max. IIH = 0.02mA max.
- Output Voltage:
  - Low: VOL = 0.5 V max. IOL = 8mA max.
  - High: VOH = 2.7V min.; IOH = 400μA

1.3.3 General Purpose Timer/Counter

- Channels: One 16-bit up/down timer/counter
- Clock Input: Internal 24MHz or external CLK input up to 20MHz

1.3.4 General Specifications

- Connector: 100-pin D-type SCSI-II connector
- Operating Temperature: 0°C to 60°C
- Storage Temperature: -20°C to 80°C
- Humidity: 5 to 95%, non-condensing
- Power Consumption:
  - +5V @ 560mA typical
  - +3.3V @ 100mA typical
- ±15V (pin 35, pin 85) output current (max.): 5mA
- +5V (pin 49, pin 99) output current (max.): 500mA
- Dimensions: Standard Compact PCI 3U size

1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW. All software options are included in the ADLINK All-in-One CD. Commercial software drivers are protected with licensing authorization codes. Without an authorization code, you can install and run the demo version for trial/demonstration purposes for up to two hours. Contact your ADLINK dealer to purchase a software license. The ADLINK Measurement, Automation & Platform Service (MAPS) is a software service package designed for data acquisition, automation and PXI platforms. By leveraging low-level kernel management and a user friendly API, users can easily manage devices under a Windows environment and focus on developing applications.

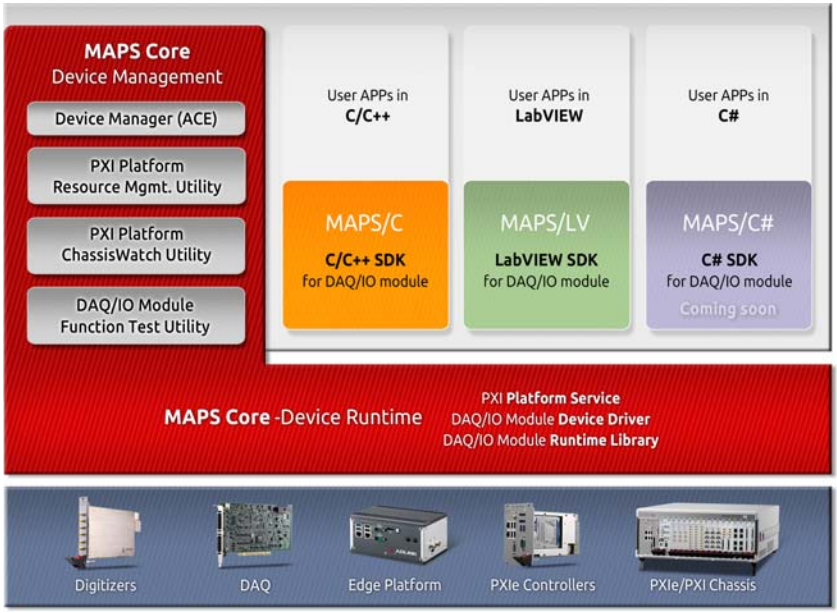

Figure 1-1: ADLINK MAPS Architecture

1.4.1 MAPS Core

ADLINK MAPS Core is a software package that includes all the device drivers for Windows and a system level management tool called ACE (ADLINK Connection Explorer). With MAPS Core installed, the operating system can identify ADLINK's devices correctly and assign the necessary resources for low-level access, such as IO read/write or direct memory access. MAPS/Core is necessary for all ADLINK DAQ modules. To ensure the user has the latest software, go to the ADLINK product webpage or contact ADLINK technical service.

MAPS Core also comes with a system management portal called ADLINK Connection Explorer (ACE). Through ACE, users can discover and manage ADLINK DAQ modules to, for example, reserve a certain size of memory buffer for DMA operation or set the user alias name for operating the module in a LabVIEW environment.

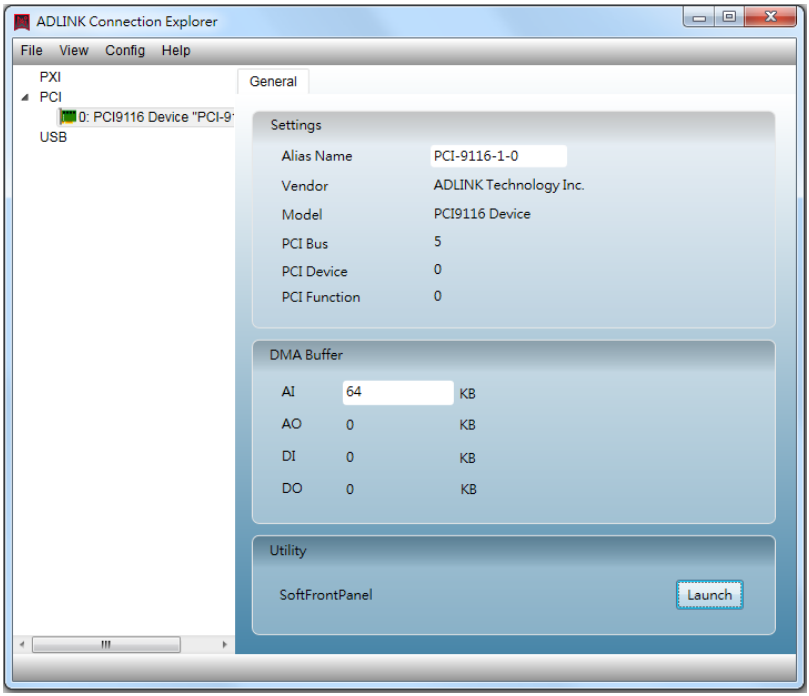

Figure 1-2: ADLINK Connection Explorer (ACE)

ADLINK Connection Explorer (ACE) also provides a ready-to-use soft-front panel for digitizer products. By clicking the Launch button in the lowest "Utility" block, this soft-front panel allows users to control digitizers through the UI and display the acquired waveform/data on the screen.

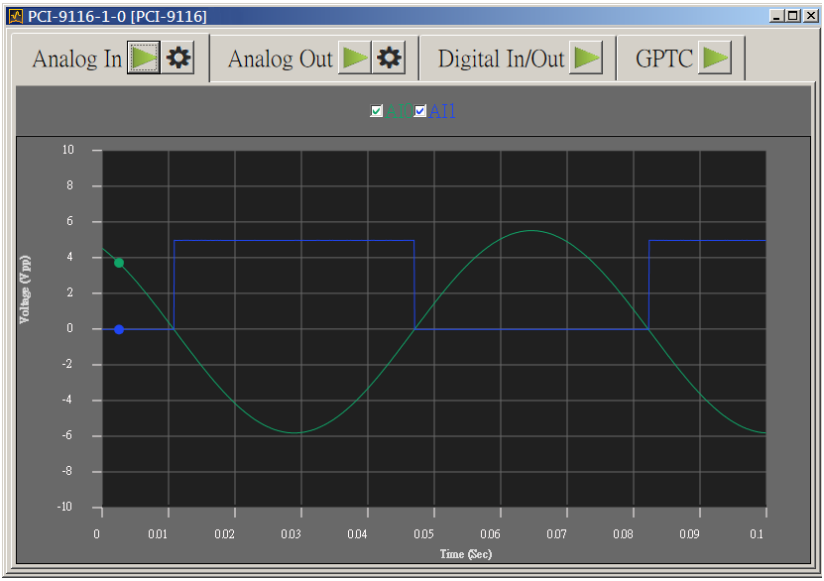

Figure 1-3: ACE Soft Front Panel

1.4.2 MAPS/LV, LabVIEW Support

For customers who develop their own programs in LabVIEW, please install the MAPS/LV software package. The MAPS/LV, also called DAQ-LabVIEW Plus, includes the software library and sample program for LabVIEW. Download and install the latest MAPS/LV software from the following website and refer to the MAPS/LV manual: https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_LV?Lang=en

1.4.3 MAPS/C, C & C++ Support

For customers who develop their own programs in C or C++ environments, install the MAPS/C software package. MAPS/C includes all the software components required for developing applications in C/C++, such as header files, a device API library and versatile sample programs for understanding how to manipulate the device correctly. Find the latest MAPS/C on the ADLINK website.

2 Installation

This chapter describes how to install the cPCI-9116 series cards. The contents of the package and unpacking information that you should be aware of are described first.

The cPCI-9116 series cards perform an automatic configuration of the IRQ, port address, and BIOS address. You do not need to set these configurations as you would in ISA form factor DAS cards. Automatic configuration allows your system to operate more reliably and safely.

2.1 What You Have

In addition to this *User's Manual*, the package should also include the following items:

- cPCI-9116 Analog Input Data Acquisition Card
- ADLINK All-in-one Compact Disc
- Software Installation Guide

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2.2 Unpacking

The card contains electro-static sensitive components that can be easily be damaged by static electricity.

Therefore, the card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handling damages on the carton before continuing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface component side up.

Again, inspect the module for damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module placed on a firm flat surface.

Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/ vendor immediately for assistance and obtain authorization before returning any product.

You are now ready to install your cPCI-9116.

2.3 cPCI-9116 Layout

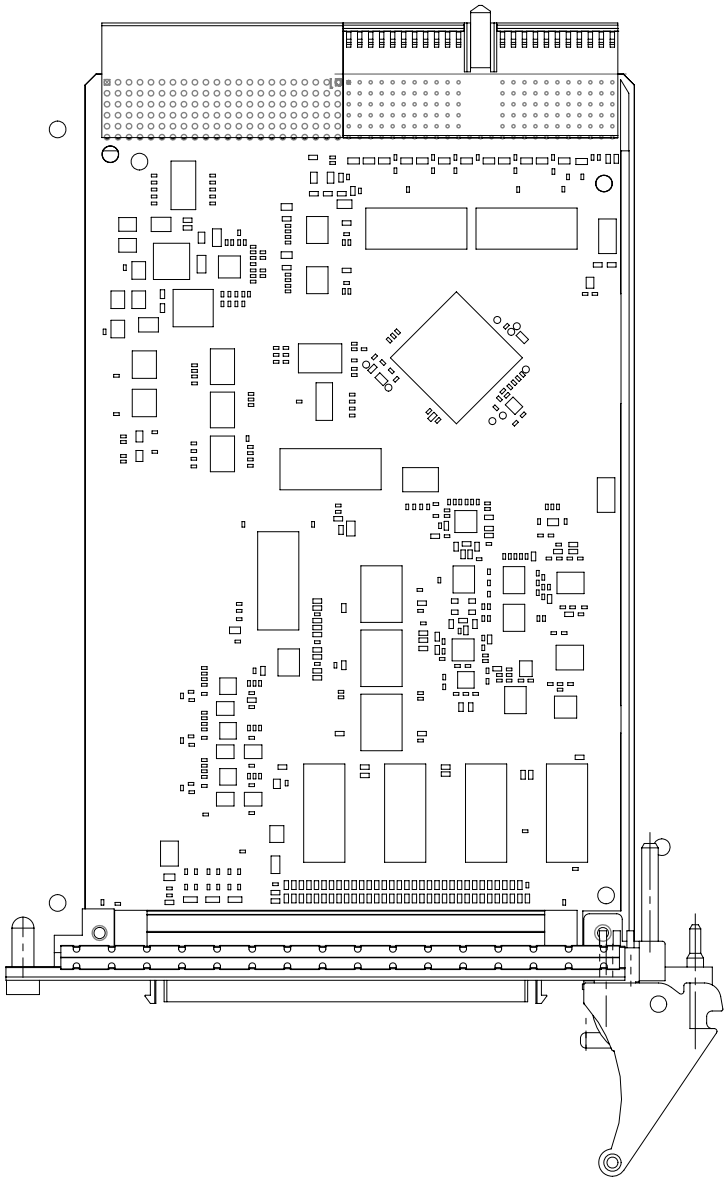

Figure 2-1: PCB Layout of the cPCI-9116

2.4 PCI Configuration

2.4.1 Plug and Play

As a plug and play component, the board requests an interrupt number via a system call. The system BIOS responds with an interrupt assignment based on the board information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load seen by the system.

2.4.2 Configuration

The board configuration is done on a board-by-board basis for all PCI form factor boards on your system. Because configuration is controlled by the system and software, there are no jumpers for base-address, DMA, and interrupt IRQ which need to be set by the user.

The configuration is subject to change with every boot of the system as boards are added or removed.

2.4.3 Troubleshooting

If your system doesn't boot or if you experience erratic operation with your PCI board in place, it's likely caused by an interrupt conflict (such as an incorrectly configured the BIOS setup). Consult the BIOS documentation that came with your system.

3 Signal Connections

This chapter describes the connectors of the cPCI-9116 series. The signal connections between the cPCI-9116 series cards and external devices are also outlined.

3.1 Connectors and Pin Assignment

The cPCI-9116 is equipped with one 100-pin SCSI-type connector (J1).

J1 is used for digital input/output, analog input, and timer/counter signals. The pin assignment for the connector is illustrated in Figure 3-1.

3.1.1 100-pin SCSI-type Connector (J1)

	U_CMMD	1	51	AGND	
AIH0	AI0	2	52	AI32	AIL0
AIH1	AI1	3	53	AI33	AIL1
AIH2	AI2	4	54	AI34	AIL2
AIH3	AI3	5	55	AI35	AIL3
AIH4	AI4	6	56	AI36	AIL4
AIH5	AI5	7	57	AI37	AIL5
AIH6	AI6	8	58	AI38	AIL6
AIH7	AI7	9	59	AI39	AIL7
AIH8	AI8	10	60	AI40	AIL8
AIH9	AI9	11	61	AI41	AIL9
AIH10	AI10	12	62	AI42	AIL10
AIH11	AI11	13	63	AI43	AIL11
AIH12	AI12	14	64	AI44	AIL12
AIH13	AI13	15	65	AI45	AIL13
AIH14	AI14	16	66	AI46	AIL14
AIH15	AI15	17	67	AI47	AIL15
AIH16	AI16	18	68	AI48	AIL16
AIH17	AI17	19	69	AI49	AIL17
AIH18	AI18	20	70	AI50	AIL18
AIH19	AI19	21	71	AI51	AIL19
AIH20	AI20	22	72	AI52	AIL20
AIH21	AI21	23	73	AI53	AIL21
AIH22	AI22	24	74	AI54	AIL22
AIH23	AI23	25	75	AI55	AIL23
AIH24	AI24	26	76	AI56	AIL24
AIH25	AI25	27	77	AI57	AIL25
AIH26	AI26	28	78	AI58	AIL26
AIH27	AI27	29	79	AI59	AIL27
AIH28	AI28	30	80	AI60	AIL28
AIH29	AI29	31	81	AI61	AIL29
AIH30	AI30	32	82	AI62	AIL30
AIH31	AI31	33	83	AI63	AIL31
	AGND	34	84	AGND	
	+15V out	35	85	-15V out	
	N/C	36	86	N/C	
	DI0	37	87	DO0	
	DI1	38	88	DO1	
	DI2	39	89	DO2	
	DI3	40	90	DO3	
	DI4	41	91	DO4	
	DI5	42	92	DO5	
	DI6	43	93	DO6	
	DI7	44	94	DO7	
	ExtTimeBase	45	95	N/C	
	ExtTrg	46	96	GP_TC_CLK	
	SSH_OUT	47	97	GP_TC_GATE	
	GP_TC_OUT	48	98	GP_TC_UPDN	
	+5V Out	49	99	+5V Out	
	DGND	50	100	DGND	

Figure 3-1: J1 Pin Assignments

3.1.2 J1 Connector Legend

Signal Name	Definition
U_CMMD	User Common Mode
AIn	Analog Input Channel n (single-ended)
AIHn	Analog High Input Channel n (differential)
AILn	Analog Low Input Channel n (differential)
DIn	Digital Input Signal Channel n
DOn	Digital Output Signal Channel n
ExtTimeBase	External Timebase Clock Input
ExtTrg	External Digital Trigger Signal
SSH_OUT	SSH Output Signal
GP_TC_CLK	General Purpose Timer/Counter Clock Input
GP_TC_GATE	General Purpose Timer/Counter Gate Input
GP_TC_UPDN	Purpose Timer/Counter Up/Down Control Input (0:down, 1:up)
GP_TC_OUT	General Purpose Timer/Counter Output
+5V OUT	+5V Output
+15V OUT	+15V Output
-15V OUT	-15V Output
AGND	Analog Ground
DGND	Digital Ground
N/C	No Connection

Table 3-1: J1 Connector Legend

3.2 Analog Input Signal Connection

The cPCI-9116 series provides up to 64 single-ended or 32 differential analog input channels. You can set and fill the channel gain queue to get the desired combination of the input signal types. The analog signals can be converted to digital values by the A/D converter. To avoid ground loops and to obtain accurate measurements from the A/D conversion, it is important to understand the signal source type and how to choose the analog input modes: Single-ended, Differential, or User Common Mode.

3.2.1 Types of Signal Sources

Floating Signal Sources

A floating signal source is not connected in any way to the building's ground system. A device with an isolated output is a floating signal source, such as optical isolator outputs, transformer outputs, and thermocouples.

Ground-Referenced Signal Sources

A ground-referenced signal is connected in some way to the building's system. That is, the signal source is already connected to a common ground point with respect to the cPCI-9116 card, assuming that the computer is plugged into the same power system. Non-isolated outputs of instruments and devices that plug into the buildings power system are ground-referenced signal sources.

3.2.2 Input Configurations

Single-ended Mode

In single-ended mode, all input signals are connected to ground provided by the cPCI-9116 card. It is suitable for connections with floating signal sources. Figure 3-2 illustrates single-ended connection. Note that when more than two floating sources are connected, these sources will be referenced to the same common ground.

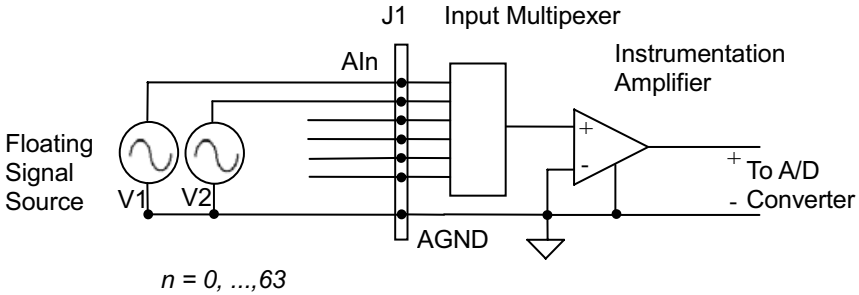

Figure 3-2: Single-ended Mode and Floating sources

Differential Input Mode

The differential input mode provides two inputs that respond to signal voltage differences between them. If the signal source is ground-referenced, the differential mode can be used for common-mode noise rejection. Figure 3-3 shows the connection of ground-referenced signal sources under differential input mode.

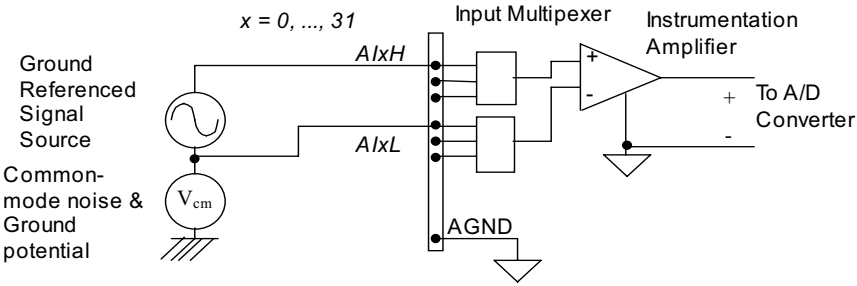

Figure 3-3: Ground-referenced source and differential input

Figure 3-4 shows how to connect a floating signal source to the cPCI-9116 card in differential input mode. For floating signal sources, a resistor is required on each channel to provide a bias return path. The resistor value should be about 100 times the equivalent source impedance. If the source impedance is less than 100 ohms, simply connect the negative side of the signal to AGND as well as the negative input of the instrumentation amplifier, without any resistors. In differential input mode, less noise is coupled into the signal connections than in single-ended mode.

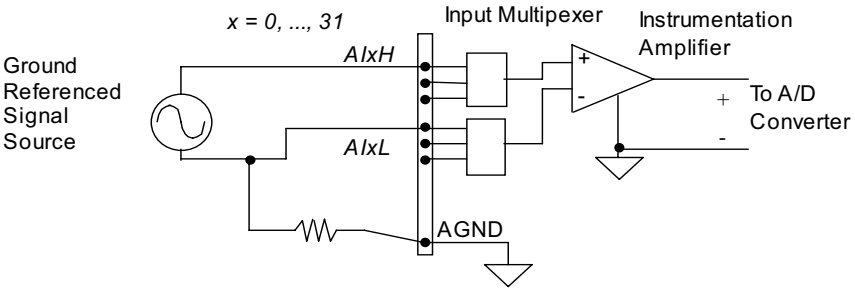

Figure 3-4: Floating source and differential input

User Common Mode (U_CMMD)

To measure ground-referenced signal sources, which are connected to the same ground point, you can connect the signals in a User-Common-Mode (U_CMMD) configuration. Figure 3-5 illustrates the connections. The signal local ground reference is connected to the negative input of the instrumentation amplifier, and the common-mode ground potential to signal ground. The instrumentation amplifier will now reject the cPCI-9116 series ground.

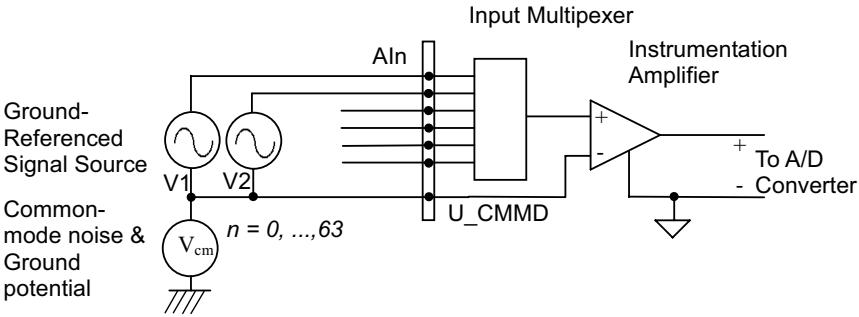

Figure 3-5: Ground-referenced source & U_CMMD connections

3.3 Digital I/O Connection

The cPCI-9116 series card provides 8 digital input and 8 digital output channels. The digital I/O signals are fully TTL/DTL compatible. The details of the digital I/O signal specification can be found in section 1.3.2.

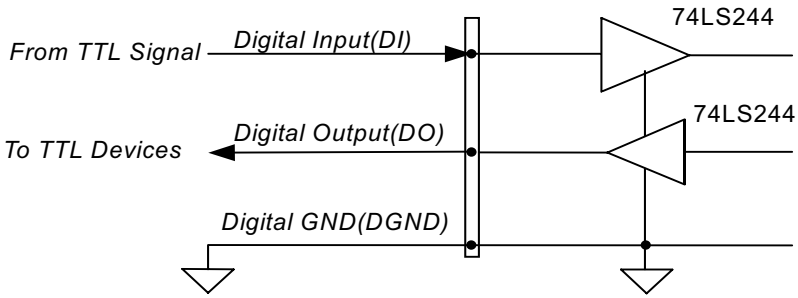

Figure 3-6: Digital I/O Connection

4 Operation Theory

The operation theory of the functions on the cPCI-9116 series is described in this chapter. The functions include the A/D conversion, Digital I/O and General Purpose Counter / Timer. The operation theory can help you better understand how to configure and program the cPCI-9116 series card.

4.1 A/D Conversion Procedure

When using an A/D converter, users should beware of the properties of the signal to be measured. Users can decide which channel to use and where to connect the signals to the card. See “Analog Input Signal Connection” on page 15. for signal connections. In addition, users should define and control the A/D signal configurations, including channels, gains, and A/D signal types.

The A/D acquisition is initiated by a trigger source; users must decide how to trigger the A/D conversion. The data acquisition will start when a trigger condition is met.

After the end of the A/D conversion, the A/D data is buffered in a Data FIFO. The A/D data is then transferred into PC's memory for further processing.

There are two acquisition modes: software polling and scan acquisition. They will be described separately in the following sections, including the timing, signal source control, trigger mode, and transfer method.

4.1.1 Conversion in Software Polling Mode

This is the easiest way to acquire a single A/D data. The A/D converter starts a conversion when the user writes 1 into bit 10 of the A/D trigger mode register. After the software initializes the A/D conversion, the software polls the FIFO ***Empty*** status (bit 4) in the A/D & FIFO Status register until it changes to active low logic.

If the Data FIFO is empty before an A/D conversion starts, the ***Empty*** bit will be high. After the A/D conversion is completed, the A/D data is written to the Data FIFO immediately, thus ***Empty*** becomes low. You can consider the ***Empty*** bit as a flag to indicate the converted data ready status. That is, a low ***Empty*** bit meaning

the data is ready. The A/D data is now ready to be transferred to host memory from the FIFO.

This method is suitable for applications that need to process AD data in real time. Under this mode, the timing of the A/D conversion is fully controlled by the software. However, it is difficult to control a fixed A/D conversion rate unless another timer interrupt service routine is used to generate a fixed conversion rate trigger.

ADLINK's software driver provides an integral function to acquire a single data (that is, it will start an A/D conversion, then poll the ***Empty*** flag and read the data back when the data is ready). We also provide individual functions to allow users to start an A/D conversion only. Users must read it back from the A/D data register by themselves. This method makes it possible to read A/D converted data without polling. The conversion and acquisition time of the ADC does not exceed 4μs. Hence, after software conversion, the software need only wait for a maximum of 4μs to read the A/D data register without polling.

4.1.2 Channel Gain Queue Configuration

In both software polling and programmable scan acquisition mode, the channel, gain, and input configuration (single-end, differential, and U_CMMD), where you want to acquire samples from, can be specified in the **Channel Gain Queue**. You can set the channel number in the Channel Gain Queue in any order. Therefore, you can control the channel order from which data is acquired with different gain and input configuration for each channel. The maximum number of entries you can set is 512 channels. The channel order of acquisition is the same as the order you set in the Channel Gain Queue. When the specified channels are sampled from the beginning to the end in the Channel Gain Queue, the channels in the Channel Gain Queue will be sampled again until the specified number of samples have been acquired.

4.2 Programmable Scan Acquisition Mode

4.2.1 Scan Timing and Procedure

It's recommended that this mode be used if your application needs a fixed and precise A/D sampling rate. You can accurately program the period between conversions of each individual channel in the scan and the period between conversions of the entire scan. There are four counters that must be specified:

SI_counter (24-bit):	Specifies the scan interval = SI_counter/ timebase
SI2_counter (16 bit):	Specifies the data sampling interval = SI2_counter/timebase
SC_counter (24 bit):	Specifies the scan count counter after trigger
DIV_counter (9 bit):	Specifies the number of samples per scan

The acquisition timing and the meaning of the four counters are illustrated in Figure 4-1.

Timebase Clock Source

In scan acquisition mode, all the A/D conversions start on the output of counters, which use **Timebase** as the clock source. With the software you can specify the timebase to be either an internal clock source (onboard 24MHz) or an external clock input on pin 45 of J1. The external clock is useful when you want to acquire data at rates not available with the internal A/D sample clock. The external clock source must generate TTL-compatible continuous clocks, and the maximum frequency is 24MHz while the minimum is 1MHz.

3 scans, 4 samples per scan (SC_Counter = 3, DIV_Counter = 4)

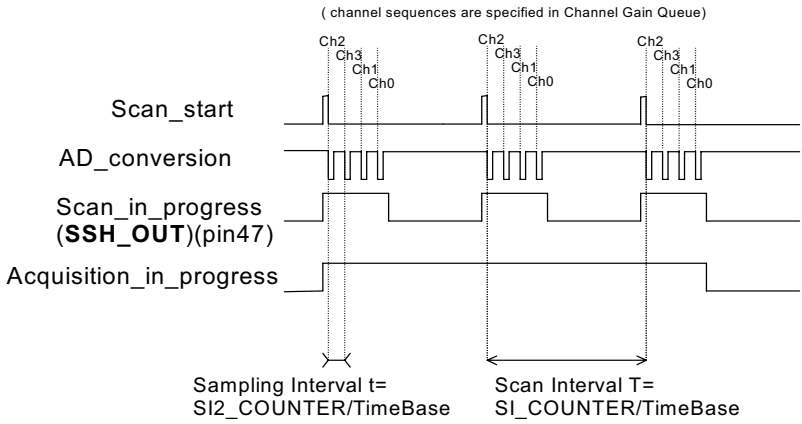

Figure 4-1: Scan Timing

In scan acquisition mode, the channel, gain, and input configurations (single-end, differential, or U_CMMD) must be specified in the hardware **Channel Gain Queue**. See “Channel Gain Queue Configuration” on page 23.

There are five trigger modes to start the scan acquisition. See “Trigger Modes” on page 24. Data transfer modes are discussed in Section 4.3 on page 33.

NOTE:

1. The maximum A/D sampling rate is 250kHz. Therefore, SI2_counter can’t be smaller than 96 while using the internal timebase.
2. The SI_counter is a 24-bit counter and the SI2_counter is a 16-bit counter. Therefore, the maximum scan interval while using the internal Timebase = 2^{24}/24M s = 0.699s, and the maximum sampling interval between 2 channels while using the internal timebase = 2^{16}/24M s = 2.73ms.
3. The scan interval can’t be smaller than the product of the data sampling interval and the DIV_counter value. The relationship can be represented as: SI_counter>=SI2_counter*DIV_counter.

Scan with SSH

You can send the SSH_OUT signal on pin 47 of J1 to external S&H circuits to sample and hold all signals if you want to simultaneously sample all channels in a scan, as illustrated in Figure 4-1.

The 'SSH_OUT' signal is sent to external S&H circuits to hold the analog signal. Users must implement external S&H circuits on their own to carry out the S&H function. There are no onboard S&H circuits.

4.2.2 Channel Gain Queue Configuration

Like software polling acquisition mode, the channel, gain, and input configurations (single-end, differential, and U_CMMD) must also be specified in the hardware **Channel Gain Queue** under scan acquisition mode. See "Channel Gain Queue Configuration" on page 20. Note that in scan acquisition mode, the number of entries in the channel gain queue is normally equivalent to the value of DIV_counter (that is, the numbers of samples per scan).

Example:

Set

SI2_counter = 240

SI_counter = 960

SC_counter = 3

DIV_counter = 4

Timebase = Internal clock source

Channel entries in the Channel Gain Queue: ch1, ch2, ch0, ch2

Then

Acquisition sequence of channels: 1, 2, 0, 2, 1, 2, 0, 2, 1, 2, 0, 2. Sampling Interval = 240/24M s = 10 us

Scan Interval = 960/24M s = 40 us Equivalent sampling rate of ch0, ch1: 25kHz Equivalent sampling rate of ch2: 50kHz

4.2.3 Trigger Modes

There are five trigger modes (software-trigger, pre-trigger, post-trigger, middle-trigger, and delay-trigger) to start the data acquisition described in Scan Timing and Procedure. All but software trigger are external digital triggers. An external digital trigger event occurs when a rising edge or a falling edge (software programmable) of a digital signal is detected on pin 46 of J1. They are described as follows.

Software-Trigger Acquisition

This trigger mode does not need any external trigger source. The data acquisition starts right after you execute the specified function calls to begin the operation. The scan timing is the same as Figure 4-1.

The total acquired data length = DIV_counter * SC_counter.

Pre-Trigger Acquisition

Use pre-trigger acquisition in applications where you want to collect data before an external trigger event. The A/D starts when you execute the specified function calls to begin the operation, and it stops when the external trigger event occurs. Users must program the value M in the **M_counter** (16-bit) to specify the amount of stored scans of data before the trigger event. If the external trigger occurs after M scans of data are converted, the program only stores the last M scans of data, as illustrated in Figure 4-2, where M_counter = M = 3, DIV_counter = 4, SC_counter = 0. The total stored amount of data = DIV_counter *M_counter = 12.

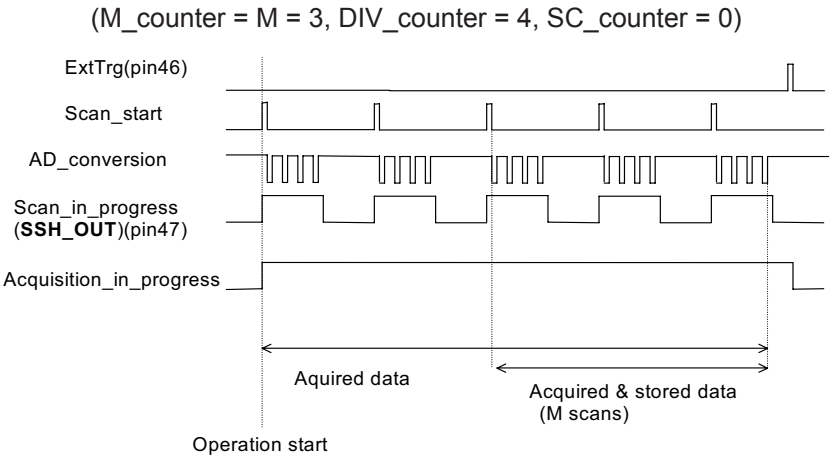

Figure 4-2: Pre-trigger (trigger occurs after M scans)

NOTE:

If an external trigger event occurs when a scan is in progress, the data acquisition won't stop until this scan completes, and the stored M scans of data include the last scan. Therefore, the first stored data will always be the first channel entry of a scan (that is, the first channel entry in the channel gain queue if the number of entries in the channel gain queue is equivalent to the value of DIV_counter), no matter when the trigger signal occurs, as illustrated in Figure 4-3, where M_counter = M =3, DIV_counter = 4, SC_counter = 0.

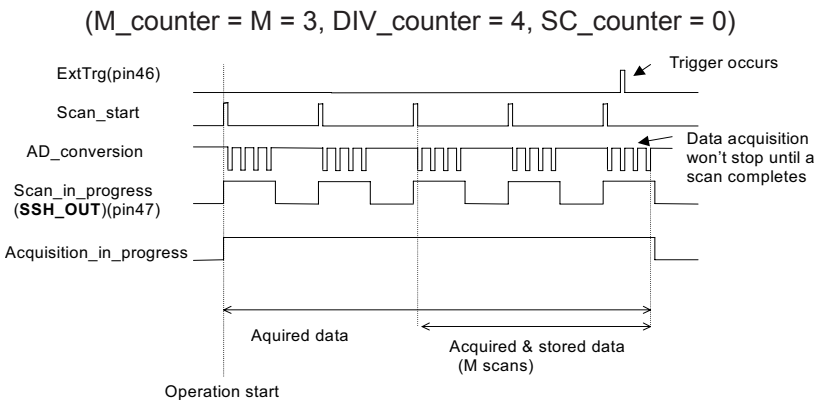

Figure 4-3: Pre-trigger (trigger with scan is in progress)

When an external trigger signal occurs before the first M scans of data are converted, the amount of stored data could be fewer than the originally specified amount of DIV_counter * M_counter, as illustrated in Figure 4-4. This situation can be avoided by setting **M_enable**. If **M_enable** is set to 1, the trigger signal will be ignored until the first M scans of data are converted, and it assures user of obtaining M scans of data under pre-trigger mode, as illustrated in Figure 4-5. However, if **M_enable** is set to 0, the trigger signal will be accepted in any time, as illustrated in Figure 4-4. Note that the total amount of stored data is still always a multiple of DIV_counter (number of samples per scan) because the data acquisition won't stop until a scan is completed.

(M_Counter = M = 3, DIV_Counter = 4, SC_Counter = 0)

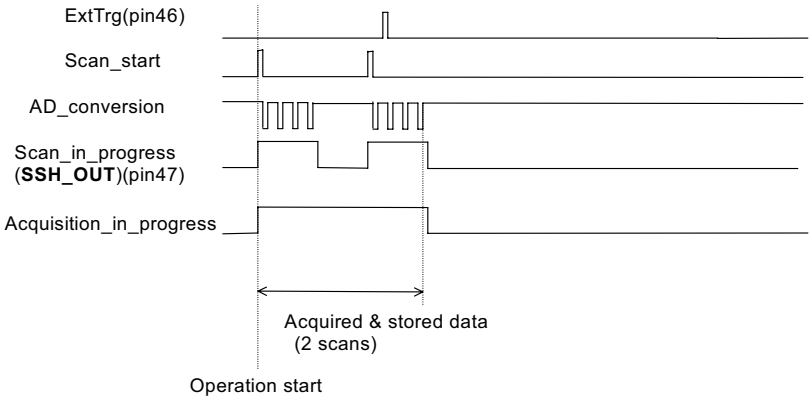

Figure 4-4: Pre-trigger with M_enable = 0 (before M scans)

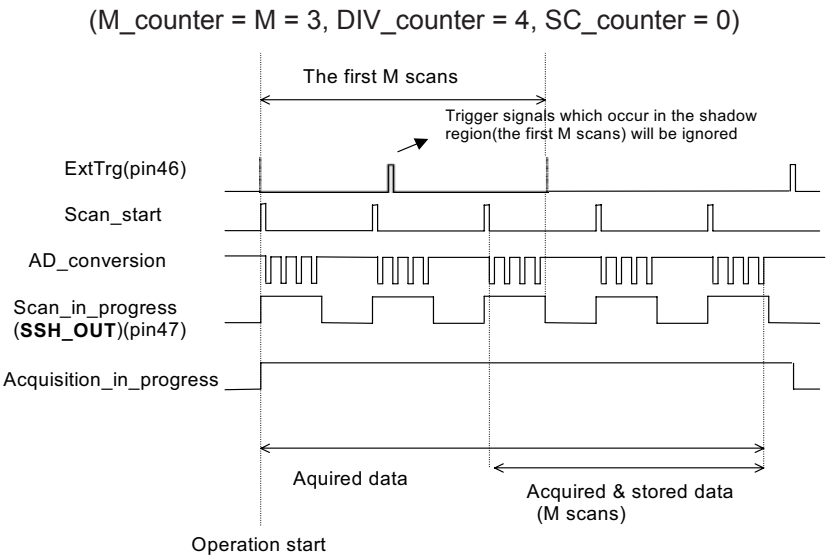

Figure 4-5: Pre-trigger with M_enable = 1

NOTE:

The SC_counter must be set to 0 in pre-trigger acquisition mode.

Middle-Trigger Acquisition

Use middle-trigger acquisition in applications where you want to collect data before and after an external trigger event. The number of scans stored before the trigger is specified in M_counter, while the number of scans after the trigger is specified in SC_counter.

Like pre-trigger mode, the number of stored data can be less than the specified amount of data (DIV_counter *(M_counter+SC_counter)) if an external trigger occurs before M scans of data is converted. The M_enable bit in middle-trigger mode takes the same effect as in pre-trigger mode. If M_enable is set to 1, the tigger signal will be ignored until the first M scans of data are converted, this assures user of obtaining M+N scans of data under middle-trigger mode.

However, if M_enable is set to 0, the trigger signal will be accepted at any time. Figure 4-6 shows the acquisition timing with M_enable = 1.

(M_Counter = M = 3, DIV_Counter = 4, SC_Counter = N = 1)

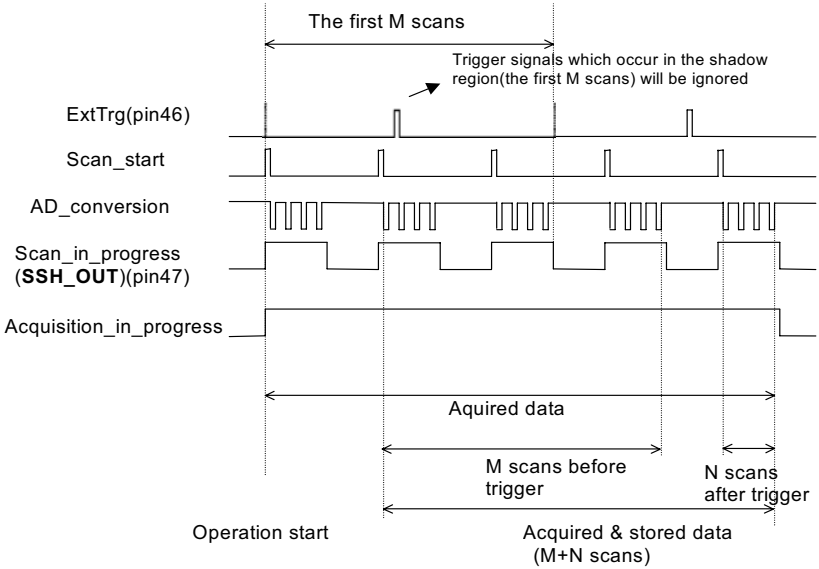

Figure 4-6: Middle trigger with M_enable = 1

If an external trigger event occurs when a scan is in progress, the stored N scans of data would include this scan. **The first stored data will always be the first channel entry of a scan**, as illustrated in Figure 4-7.

(M_Counter = M = 2, DIV_Counter = 4, SC_Counter = N = 2)

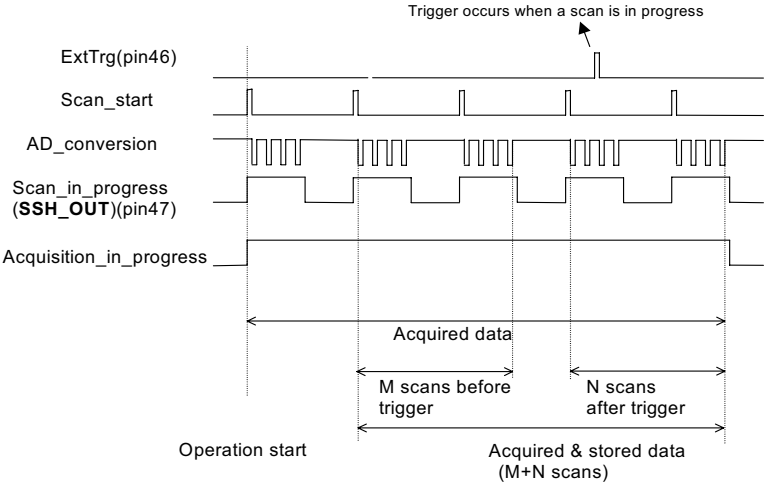

Figure 4-7: Middle trigger (trigger with scan is in progress)

Post-Trigger Acquisition

Use post-trigger acquisition in applications where you want to collect data after an external trigger event. The number of scans after the trigger is specified in SC_counter, as illustrated in Figure 4-8. The total acquired data length = DIV_counter * SC_counter.

(DIV_Counter = 4, SC_Counter = 3)

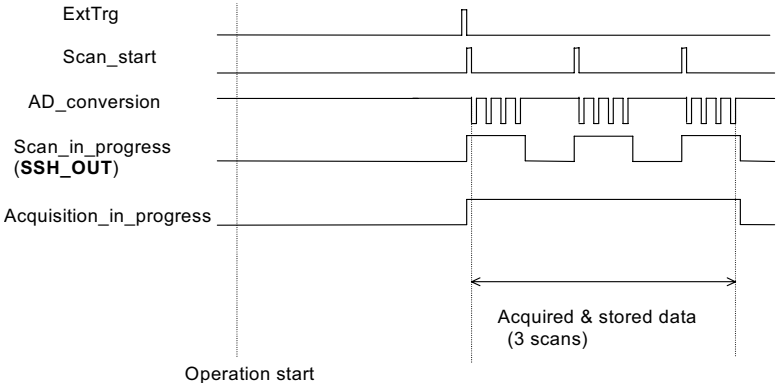

Figure 4-8: Post trigger

Delay Trigger Acquisition

Use delay trigger acquisition in applications where you want to delay the data collection after the occurrence of a specified trigger event. The delay time is controlled by the value, which is pre-loaded in the **Delay_counter** (16-bit). The counter counts down on the rising edge of Delay_counter clock source after the trigger condition is met. The clock source can be software programmed either timebase clock (24MHz) or A/D sampling clock (Timebase/ SI2_counter). When the count reaches 0, the counter stops and the cPCI-9116 card starts to acquire data. The total acquired data length = DIV_counter * SC_counter.

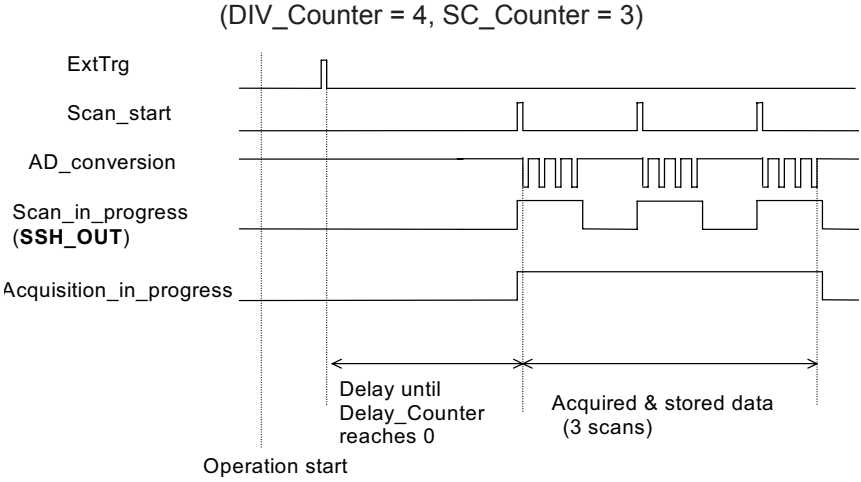

Figure 4-9: Delay trigger

NOTE:

When the Delay_counter clock source is set to Timebase, the maximum delay time = 2^{16}/24M s = 2.73ms, and when the source is set to A/D sampling clock, the maximum delay time = 2^{16} * SI2_counter / 24M.

Post-Trigger or Delay-trigger Acquisition with Re-trigger

Use post-trigger or delay-trigger acquisition with re-trigger function in applications where you want to collect data after several external trigger events. The number of scans after each trigger is specified in SC_counter, and users can program **Retrig_no** to specify the number of re-triggers. Figure 4-10 illustrates an example. In this example, two scans of data are acquired after the first trigger signal, then the board waits for the re-trigger signal (re-trigger signals which occur before the first two scans of data are acquired will be ignored). When the re-trigger signal occurs, the board scans two more scans of data. The process repeats until the specified amount of re-trigger signals are detected. The total acquired data length = DIV_counter * SC_counter * Retrig_no.

(DIV_Counter = 4, SC_Counter = 2, retrig_no = 3)

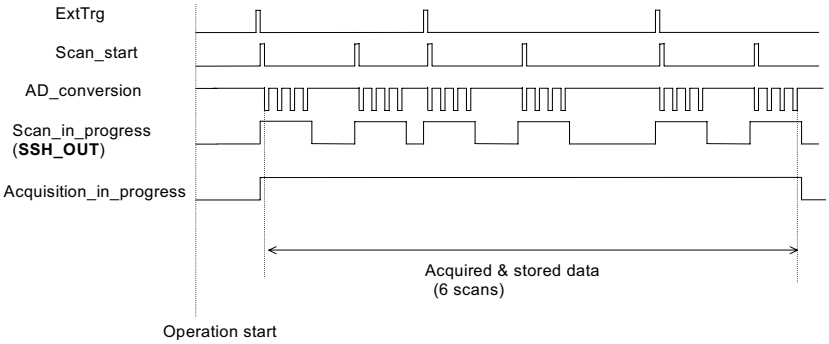

Figure 4-10: Post trigger with re-trigger

4.3 A/D Data Transfer Modes

After the end of the A/D conversion, A/D data are buffered into the **Data FIFO** memory. The FIFO size on the cPCI-9116 series card is 1024 (1K) words. If the sampling rate is 10 KHz, the FIFO can buffer 102.4 ms of analog signal. After the FIFO is full, any data after this time will be lost.

The data must be transferred to the host memory after the data is ready and before the FIFO is full. In scan acquisition mode, there are three data transfer modes that can be used.

EOC Interrupt Transfer

The cPCI-9116 series card provides traditional hardware End-Of-Conversion (EOC) interrupt capability. Under this mode, an interrupt signal is generated when the A/D conversion has ended and the data is ready to be read into the Data FIFO. The hardware interrupt will be asserted and its corresponding ISR (Interrupt Service Routine) will be invoked and executed. The ISR program can read the converted data. This method is suitable for data processing applications under real-time and a fixed sampling rate.

FIFO Half-Full Interrupt Transfer

Sometimes, the application does not need real-time processing, as the foreground program is busy polling the FIFO data. The FIFO half-full interrupt transfer mode is useful for the situation mentioned above.

Under this mode, an interrupt signal is generated when FIFO becomes half-full. It means that there are 512 words of data in the FIFO ready for transfer. The ISR can read the whole block of data when the interrupt occurs. A block is 512 words long.


NOTE:

In the current version, EOC & FIFO half-full interrupt transfer mode doesn't support pre-trigger and middle-trigger mode data acquisition. Users must use DMA transfer to work with pre-trigger or middle-trigger data acquisition.

DMA Transfer

PCI bus-mastering DMA is necessary for high speed DAQ in order to utilize the maximum PCI bandwidth. The bus-mastering controller, which is built-in into the PCI controller, controls the PCI bus

when it becomes the master on the bus. Bus mastering reduces the size of the onboard memory and reduces the CPU loading because data is directly transferred to the computer's memory without host CPU intervention.

Bus-mastering DMA provides the fastest data transfer rates on the PCI-bus. Once the analog input operation starts, control returns to your program. The hardware temporarily stores the acquired data in the onboard Data FIFO and then transfers the data to a user-defined DMA buffer memory in the computer. Note that even when the acquired data length is less than the Data FIFO, the AD data will not held in the Data FIFO but directly transferred to the host memory by bus-mastering DMA.


NOTE:

In DMA transfer mode, the maximum acquired data length in one acquisition can be up to 64M bytes (32M samples), which is the limit of the PCI controller. However, the memory that you allocate for data transfer must be continuous.

4.4 Digital Input and Output

To program digital I/O operations is fairly straightforward. The digital input (DI) operation reads data from its corresponding registers, and the digital output (DO) operation writes data to its corresponding registers. The DO can be read back when reading the DI port. Note that the DIO data channel can only be read or written to in the form of 16-bit blocks. It is impossible to access individual bits.

4.5 General Purpose Timer/Counter Operation

An independent 16-bit up/down timer/counter is designed in the FPGA for user applications. Figure 4-11 shows a simplified model of the timer/counter on the cPCI-9116 series card. It has the following features:

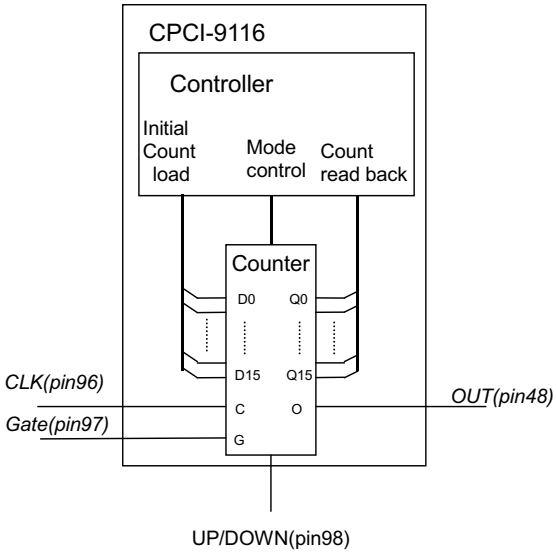

Figure 4-11: General-purpose Timer/Counter model

- Count up/count down controlled by hardware or software (low or 0: counts down, high or 1: counts up)
- Programmable counter CLK source selection (internal 24MHz or external CLK input up to 20MHz)
- Programmable gate selection (Internal or external. For internal control, you can disable counting only by software. For external gate control, either software or setting Gate = low on pin 97 of J1 disables the counting.)
- Initial count can be loaded from software
- Current count value can be read with software without affecting circuit operation
- Two programmable timer modes are provided:

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting, as illustrated in Figure 4-12. After the initial count is written, OUT is initially low, and will remain low until the counter counts to zero. OUT then goes high and will remain high until a new count is written into the counter. Counting up by software selection is invalid, but counting down is valid.

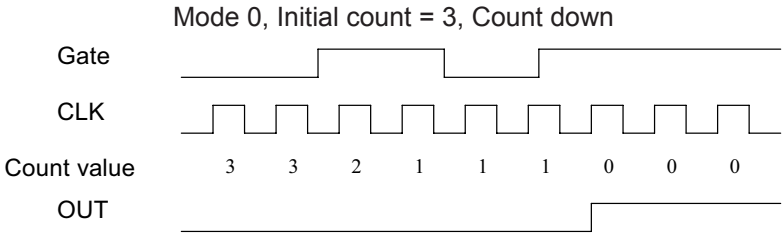

Figure 4-12: Mode 0 Operation

Mode 1: Rate Generator

This mode operates like a divide-by-N counter, as illustrated in Figure 4-13. After the initial count is written, initially OUT is low. When the counter reaches 1, OUT goes high for one clock pulse. OUT then goes low again. The counter reloads the initial count and the process will be repeated.

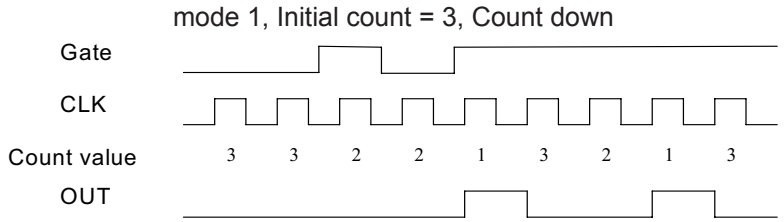

Figure 4-13: Mode 1 Operation

NOTE: In Mode 1 the initial count value N must be larger than one.

Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully
- Keep the User's Manual for future reference
- Read the Specifications section of this manual for detailed information on the recommended operating environment
- The device can be operated at an ambient temperature of 50ºC
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing:
  - Turn off power and unplug any power cords/cables
  - Reinstall all chassis covers before restoring power
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources
  - Keep device away from high heat or humidity
  - Keep device properly ventilated (do not block or cover ventilation openings)
  - Always use recommended voltage and power source settings
  - Always install and operate device near an easily accessible electrical outlet
  - Secure the power cord (do not place any object on/over the power cord)
  - Only install/attach and operate device on stable surfaces and/or recommended mountings
- If the device will not be used for long periods of time, turn off and unplug from its power source

- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location

	**BURN HAZARD** Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching. ***RISQUE DE BRÛLURES*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures.* *Pour éviter tout danger, laissez la surface refroidir avant de la toucher.*

Getting Service

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ADLINK Technology, Inc.
9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
5215 Hellyer Avenue, #110
San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
300 Fang Chun Rd., Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology GmbH
Hans-Thoma-Straße 11
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

Please visit the Contact page at www.adlinktech.com for information on how to contact the ADLINK regional office nearest you.