NI 625*x* Specifications

Specifications listed below are typical at 25 °C unless otherwise noted.

Analog Input

Number of channels

- NI 6250/NI 6251 ..... 8 differential or 16 single ended
- NI 6254/NI 6259 ..... 16 differential or 32 single ended

ADC resolution ..... 16 bits

DNL ..... No missing codes guaranteed

INL ..... Refer to the *AI Absolute Accuracy Table*

Sampling rate

- Maximum ..... 1.25 MS/s single channel, 1.00 MS/s multi-channel (aggregate)
- Minimum ..... 0 S/s
- Timing accuracy ..... 50 ppm of sample rate
- Timing resolution ..... 50 ns

Input coupling ..... DC

Input range ..... ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V, ±0.1 V

Maximum working voltage for analog inputs (signal + common mode) ..... ±11 V of AI GND

CMRR (DC to 60 Hz) ..... 100 dB

Input impedance

- Device on
  - AI+ to AI GND ..... >10 GΩ in parallel with 100 pF
  - AI– to AI GND ..... >10 GΩ in parallel with 100 pF
- Device off
  - AI+ to AI GND ..... 820 Ω
  - AI– to AI GND ..... 820 Ω

Input bias current ..... ±100 pA

Crosstalk (at 100 kHz)

- Adjacent channels ..... –75 dB
- Non-adjacent channels ..... –95 dB

Small signal bandwidth (–3 dB) ..... 1.7 MHz

Input FIFO size ..... 4,095 samples

Scan list memory ..... 4,095 entries

Data transfers ..... DMA (scatter-gather), interrupts, programmed I/O

Overvoltage protection (AI <0..31>, AI SENSE, AI SENSE 2)

- Device on ..... ±25 V for up to four AI pins
- Device off ..... ±15 V for up to four AI pins

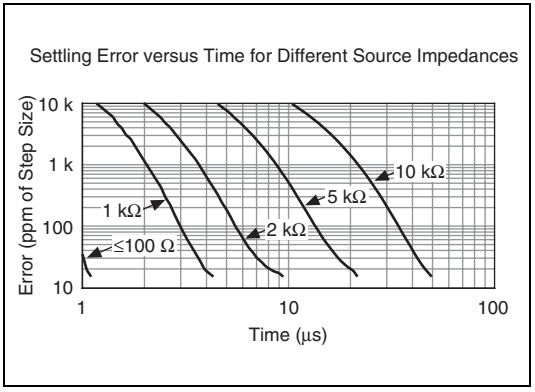
Input current during overvoltage condition ..... ±20 mA max/AI pin

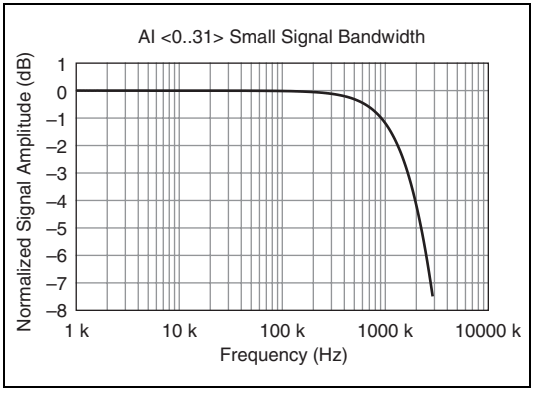
Settling Time for Multichannel Measurements

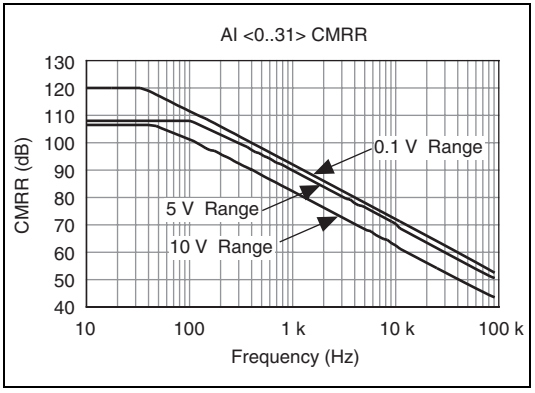
Range	±60 ppm of Step (±4 LSB for Full Scale Step)	±15 ppm of Step (±1 LSB for Full Scale Step)
±10 V, ±5 V, ±2 V, ±1 V	1 µs	1.5 µs
±0.5 V	1.5 µs	2 µs
±0.2 V, ±0.1 V	2 µs	8 µs

NATIONAL INSTRUMENTS

Typical Performance Graphs







Analog Triggers

Number of triggers 1

Source

NI 6250/NI 6251 ..... AI <0..15>, APFI 0

NI 6254/NI 6259 ..... AI <0..31>, APFI <0..1>

Functions ..... Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase

Source level

AI <0..31> ..... ±full scale

APFI <0..1> ..... ±10 V

Resolution ..... 10 bits, 1 in 1,024

Modes ..... Level triggering, level triggering with hysteresis, window triggering

Bandwidth (–3 dB)

AI <0..31> ..... 3.4 MHz

APFI <0..1> ..... 3.9 MHz

Accuracy ..... ±1%

APFI <0..1> characteristics

Input impedance ..... 10 kΩ

Coupling ..... DC

Protection

Power on ..... ±30 V

Power off ..... ±15 V

Analog Output

Number of channels

- NI 6250 0
- NI 6251 2
- NI 6254 0
- NI 6259 4

DAC resolution ..... 16 bits

DNL ..... ±1 LSB

Monotonicity ..... 16 bit guaranteed

Accuracy ..... Refer to the *AO Absolute Accuracy Table*

Maximum update rate

- 1 channel ..... 2.86 MS/s
- 2 channels ..... 2.00 MS/s
- 3 channels ..... 1.54 MS/s
- 4 channels ..... 1.25 MS/s

Timing accuracy ..... 50 ppm of sample rate

Timing resolution ..... 50 ns

Output range ..... ±10 V, ±5 V, ±external reference on APFI <0..1>

Output coupling ..... DC

Output impedance ..... 0.2 Ω

Output current drive ..... ±5 mA

Overdrive protection ..... ±25 V

Overdrive current ..... 20 mA

Power-on state ..... ±5 mV

Power-on glitch ..... 1.5 V peak for 1.5 s

Output FIFO size ..... 8,191 samples shared among channels used

Data transfers ..... DMA (scatter-gather), interrupts, programmed I/O

AO waveform modes:

- Non-periodic waveform
- Periodic waveform regeneration mode from onboard FIFO
- Periodic waveform regeneration from host buffer including dynamic update

Settling time, full scale step

15 ppm (1 LSB) ..... 2 µs

Slew rate ..... 20 V/µs

Glitch energy at midscale transition, ±10 V range

- Magnitude ..... 10 mV
- Duration ..... 1 µs

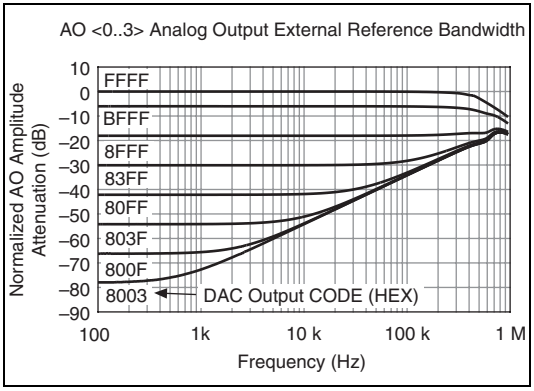
External Reference

APFI <0..1> characteristics

- Input impedance ..... 10 kΩ
- Coupling ..... DC
- Protection
  - Power on ..... ±30 V
  - Power off ..... ±15 V

Range ..... ±11 V

Slew rate ..... 20 V/µs



Calibration (AI and AO)

Recommended warm-up time ..... 15 minutes

Calibration interval ..... 2 years

AI Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Random Noise, σ (μVrms)	Absolute Accuracy at Full Scale[1] (μV)	Sensitivity[2] (μV)
Positive Full Scale	Negative Full Scale									
10	–10	60	13	1	20	21	60	280	1,920	112.0
5	–5	70	13	1	20	21	60	140	1,010	56.0
2	–2	70	13	1	20	24	60	57	410	22.8
1	–1	80	13	1	20	27	60	32	220	12.8
0.5	–0.5	90	13	1	40	34	60	21	130	8.4
0.2	–0.2	130	13	1	80	55	60	16	74	6.4
0.1	–0.1	150	13	1	150	90	60	15	52	6.0

Accuracies listed are valid for up to two years from the device external calibration.

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

GainError = ResidualAIGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualAIOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

$$\text{NoiseUncertainty} = \frac{\text{RandomNoise} \cdot 3}{\sqrt{100}}$$ For a coverage factor of 3 σ and averaging 100 points.

[1] Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

TempChangeFromLastExternalCal = 10 °C

TempChangeFromLastInternalCal = 1 °C

number_of_readings = 100

CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

GainError = 60 ppm + 13 ppm · 1 + 1 ppm · 10 GainError = 83 ppm

OffsetError = 20 ppm + 21 ppm · 1 + 60 ppm OffsetError = 101 ppm

$$\text{NoiseUncertainty} = \frac{275\ \mu\text{V} \cdot 3}{\sqrt{100}}$$ NoiseUncertainty = 83 μV

AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty AbsoluteAccuracy = 1920 μV

[2] Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

AO Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale[1] (μV)
Positive Full Scale	Negative Full Scale							
10	–10	75	17	1	40	2	64	2,080
5	–5	85	8	1	40	2	64	1,045

[1] Absolute Accuracy at full scale numbers is valid immediately following internal calibration and assumes the device is operating within 10 °C of the last external calibration. Accuracies listed are valid for up to two years from the device external calibration.

AbsoluteAccuracy = OutputValue · (GainError) + Range · (OffsetError)
GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)
OffsetError = ResidualOffsetError + AOOffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

Digital I/O/PFI

Static Characteristics

Number of channels
- NI 6250/NI 6251 ..... 24 total, 8 (P0.<0..7>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
- NI 6254/NI 6259 ..... 48 total, 32 (P0.<0..31>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
- Ground reference ..... D GND

Direction control ..... Each terminal individually programmable as input or output

Pull-down resistor ..... 50 kΩ typ, 20 kΩ min

Input voltage protection[1] ..... ±20 V on up to two pins

Waveform Characteristics (Port 0 Only)

Terminals used
- NI 6250/NI 6251 ..... Port 0 (P0.<0..7>)
- NI 6254/NI 6259 ..... Port 0 (P0.<0..31>)

Port/sample size
- NI 6250/NI 6251 ..... Up to 8 bits
- NI 6254/NI 6259 ..... Up to 32 bits

Waveform generation (DO) FIFO ... 2,047 samples

Waveform acquisition (DI) FIFO .... 2,047 samples

DI Sample Clock frequency ..... 0 to 10 MHz

DO Sample Clock frequency
- Regenerate from FIFO ..... 0 to 10 MHz
- Streaming from memory ..... 0 to 10 MHz system dependent[2]

DO or DI Sample Clock source[3] ..... Any PFI, RTSI, AI Sample or Convert Clock, AO Sample Clock, Ctr *n* Internal Output, and many other signals

PFI/Port 1/Port 2 Functionality

Functionality ..... Static digital input, static digital output, timing input, timing output

Timing output sources ..... Many AI, AO, counter, DI, DO timing signals

Debounce filter settings ..... 125 ns, 6.425 µs, 2.54 ms, disable; high and low transitions; selectable per input

Recommended Operation Conditions

Level	Min	Max
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V
Output high current (I_{OH})		
P0.<0..31>	—	–24 mA
PFI <0..15>/P1/P2	—	–16 mA
Output low current (I_{OL})		
P0.<0..31>	—	24 mA
PFI <0..15>/P1/P2	—	16 mA

Electrical Characteristics

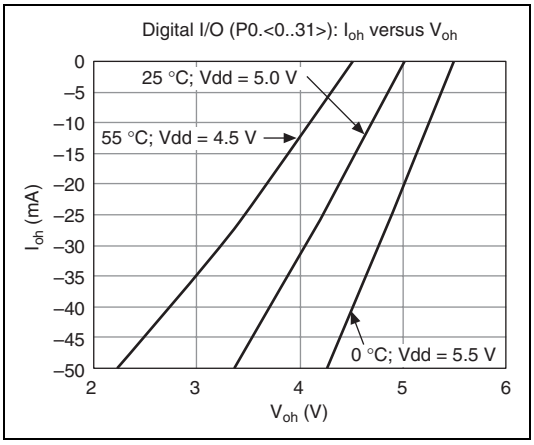
Level	Min	Max
Positive-going threshold (VT+)	—	2.2 V
Negative-going threshold (VT–)	0.8 V	—
Delta VT hysteresis (VT+ – VT–)	0.2 V	—
I_{IL} input low current (V_{in} = 0 V)	—	–10 µA
I_{IH} input high current (V_{in} = 5 V)	—	250 µA

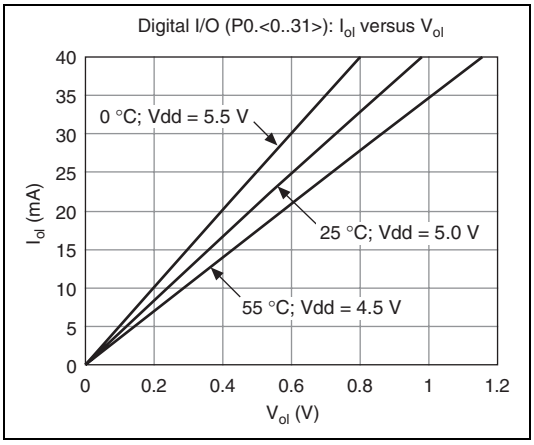
[1] Stresses beyond those listed under *Input voltage protection* may cause permanent damage to the device.

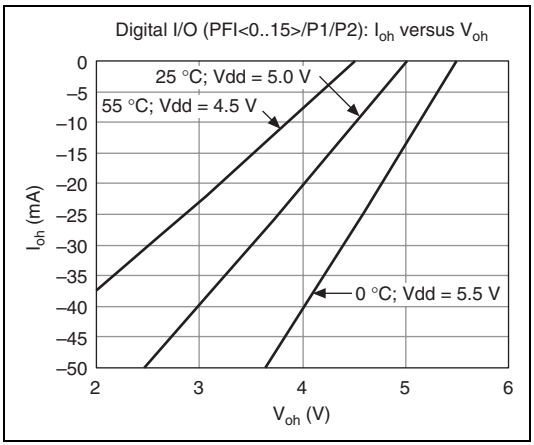
[2] Performance can be dependent on latency of bus.

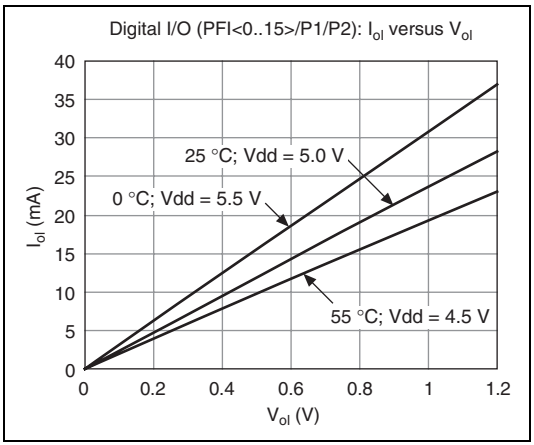
[3] The digital subsystem does not have its own dedicated internal timing engine. Therefore, a sample clock must be provided from another subsystem on the device or an external source.

Digital I/O Characteristics









General-Purpose Counter/Timers

Number of counter/timers 2

Resolution ..... 32 bits

Counter measurements ..... Edge counting, pulse, semi-period, period, two-edge separation

Position measurements ..... X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding

Output applications ..... Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling

Internal base clocks ..... 80 MHz, 20 MHz, 0.1 MHz

External base clock frequency ..... 0 MHz to 20 MHz

Base clock accuracy ..... 50 ppm

Inputs ..... Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down

Routing options for inputs ..... Any PFI, RTSI, PXI_TRIG, PXI_STAR, analog trigger, many internal signals

FIFO ..... 2 samples

Data transfers ..... Dedicated scatter-gather DMA controller for each counter/timer; interrupts; programmed I/O

Frequency Generator

Number of channels 1

Base clocks ..... 10 MHz, 100 kHz

Divisors ..... 1 to 16

Base clock accuracy ..... 50 ppm

Output can be available on any PFI or RTSI terminal.

Phase-Locked Loop (PLL)

Number of PLLs 1

Reference signal ..... PXI_STAR, PXI_CLK10, RTSI <0..7>

Output of PLL ..... 80 MHz Timebase; other signals derived from 80 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source ..... Any PFI, RTSI, PXI_TRIG, PXI_STAR

Polarity ..... Software-selectable for most signals

Analog input function ..... Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase

Analog output function ..... Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Counter/timer functions ..... Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down

Digital waveform generation (DO) function ..... Sample Clock

Digital waveform acquisition (DI) function ..... Sample Clock

Device-To-Device Trigger Bus

PCI devices ..... RTSI <0..7>[1]

PXI devices ..... PXI_TRIG <0..7>, PXI_STAR

Output selections ..... 10 MHz Clock; frequency generator output; many internal signals

Debounce filter settings ..... 125 ns, 6.425 µs, 2.54 ms, disable; high and low transitions; selectable per input

[1] In other sections of this document, *RTSI* refers to RTSI <0..7> for PCI or PCI Express devices or PXI_TRIG <0..7> for PXI devices.

Bus Interface

PCI or PXI ..... 3.3 V or 5 V signal environment

PCI Express

- Form factor ..... x1 PCI Express, specification v1.0a compliant
- Slot compatibility ..... x1, x4, x8, and x16 PCI Express slots[1]

DMA channels ..... 6, analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1

Power Requirements

Current draw from bus during no-load condition[2]

- PCI or PXI
  - +5 V ..... 0.03 A
  - +3.3 V ..... 0.725 A
  - +12 V ..... 0.35 A
- PCI Express
  - +3.3 V ..... 0.925 A
  - +12 V ..... 0.35 A

Current draw from bus during AI and AO overvoltage condition[2]

- PCI or PXI
  - +5 V ..... 0.03 A
  - +3.3 V ..... 1.2 A
  - +12 V ..... 0.38 A
- PCI Express
  - +3.3 V ..... 1.4 A
  - +12 V ..... 0.38 A

Power Limits

Caution Exceeding the power limits may cause unpredictable behavior by the device and/or PC/chassis.

PCI

- +5 V terminal (connector 0)..... 1 A max[3]
- +5 V terminal (connector 1)..... 1 A max[3]

PCI Express

- Without disk drive power connector installed
  - +5 V terminals combined ..... 0.35 A max[3]
  - P0/PFI/P1/P2 and +5 V terminals combined ..... 0.39 A max
- With disk drive power connector installed
  - +5 V terminal (connector 0) ... 1 A max[3]
  - +5 V terminal (connector 1) ... 1 A max[3]
  - P0/PFI/P1/P2 combined ..... 0.39 A max

PXI

- +5 V terminal (connector 0)..... 1 A max[3]
- +5 V terminal (connector 1)..... 1 A max[3]
- P0/PFI/P1/P2 and +5 V terminals combined..... 2 A max

Physical Requirements

Printed circuit board dimensions

- NI PCI-6250/6251/6254/6259 .... 9.7 cm × 15.5 cm (3.8 in. × 6.1 in.)
- NI PCIe-6251/6259..... 9.9 cm × 16.8 cm (3.9 in. × 6.6 in.) (half-length)
- NI PXI-6250/6251/6254/6259 .... Standard 3U PXI

Weight

- NI PCI-6250..... 142 g (5.0 oz)
- NI PCI-6251..... 149 g (5.2 oz)
- NI PCI-6254..... 152 g (5.3 oz)
- NI PCI-6259..... 162 g (5.6 oz)
- NI PCIe-6251..... 161 g (5.7 oz)
- NI PCIe-6259..... 175 g (6.1 oz)
- NI PXI-6250 ..... 212 g (7.5 oz)
- NI PXI-6251 ..... 222 g (7.8 oz)
- NI PXI-6254 ..... 222 g (7.8 oz)
- NI PXI-6259 ..... 233 g (8.2 oz)

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[1] Some motherboards reserve the x16 slot for graphics use. For guidelines on PCI Express, refer to `ni.com/pciexpress`.

[2] Does not include P0/PFI/P1/P2 and +5 V terminals.

[3] Has a self-resetting fuse that opens when current exceeds this specification.

I/O connector

NI 6250/NI 6251 .....1 68-pin VHDCI

NI 6254/NI 6259 .....2 68-pin VHDCI

Disk drive power connector
(PCI Express) .....Standard ATX peripheral connector (not serial ATA)

Maximum Working Voltage[1]

NI 6250/NI 6251/NI 6254/NI 6259
Channel to earth.....11 V, Measurement Category I

Caution Do *not* use for measurements within Categories II, III, or IV.

Environmental

Operating temperature

PCI/PXI.....0 to 55 °C

PCI Express.....0 to 50 °C

Storage temperature.....–20 to 70 °C

Humidity.....10 to 90% RH, noncondensing

Maximum altitude .....2,000 m

Pollution Degree
(indoor use only) 2

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1
- CAN/CSA-C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

Emissions ..... EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Immunity..... EN 61326:1997 + A2:2001, Table 1

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive
(safety) 73/23/EEC

Electromagnetic Compatibility
Directive (EMC) 89/336/EEC

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

[1] *Maximum working voltage* refers to the signal voltage plus the common-mode voltage.

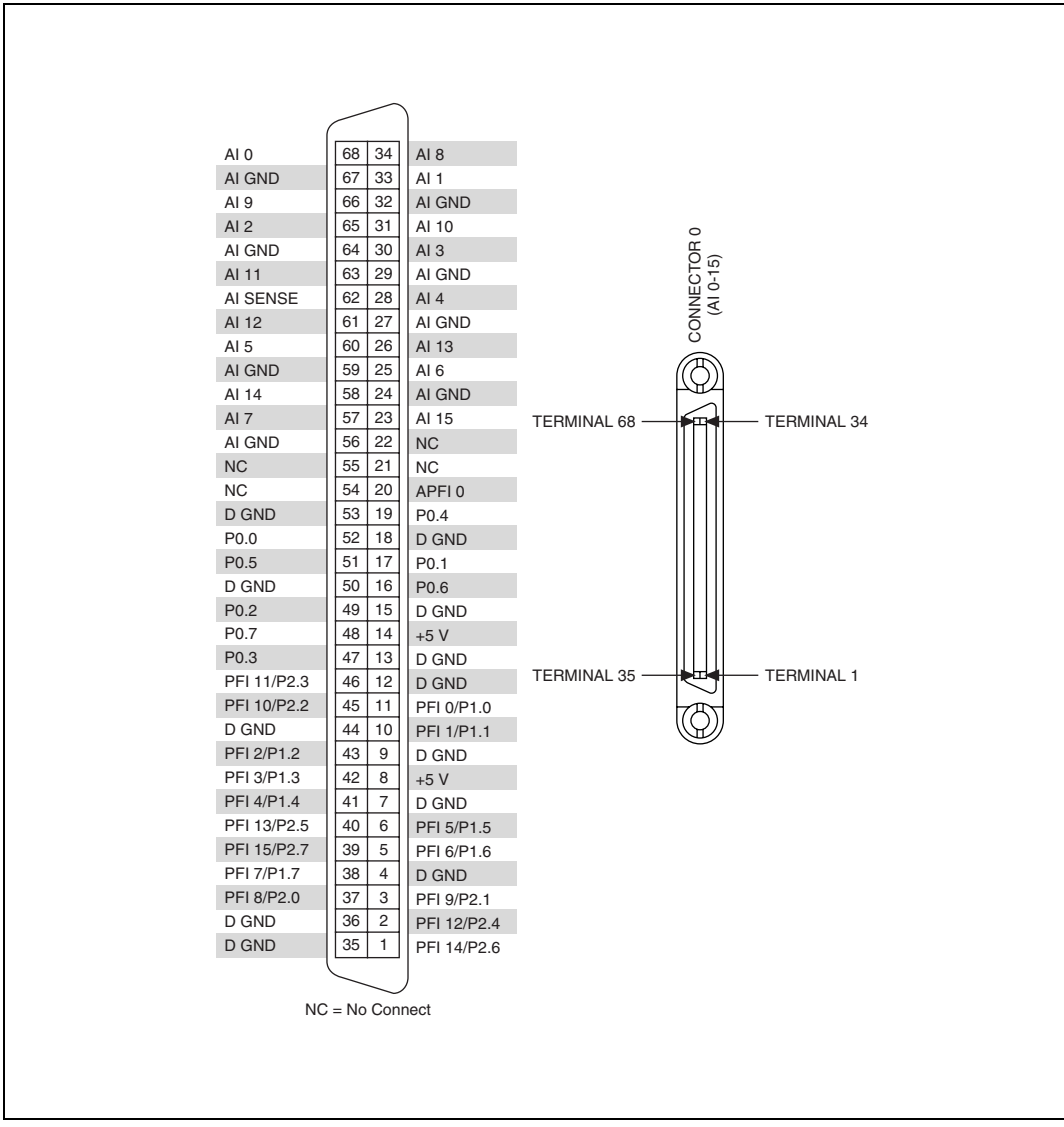

Figure 1. NI 6250 Pinout

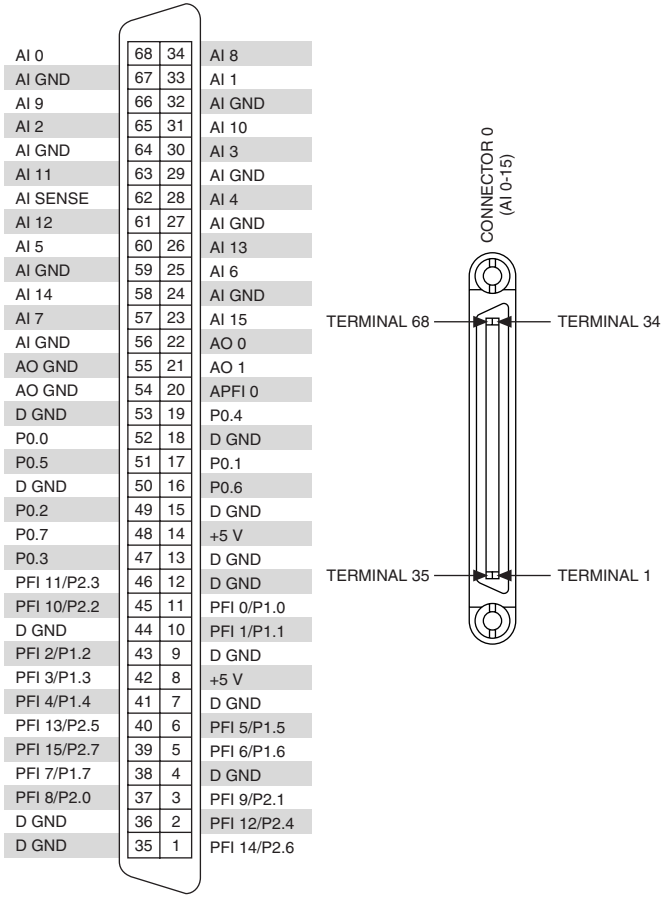

Figure 2. NI 6251 Pinout

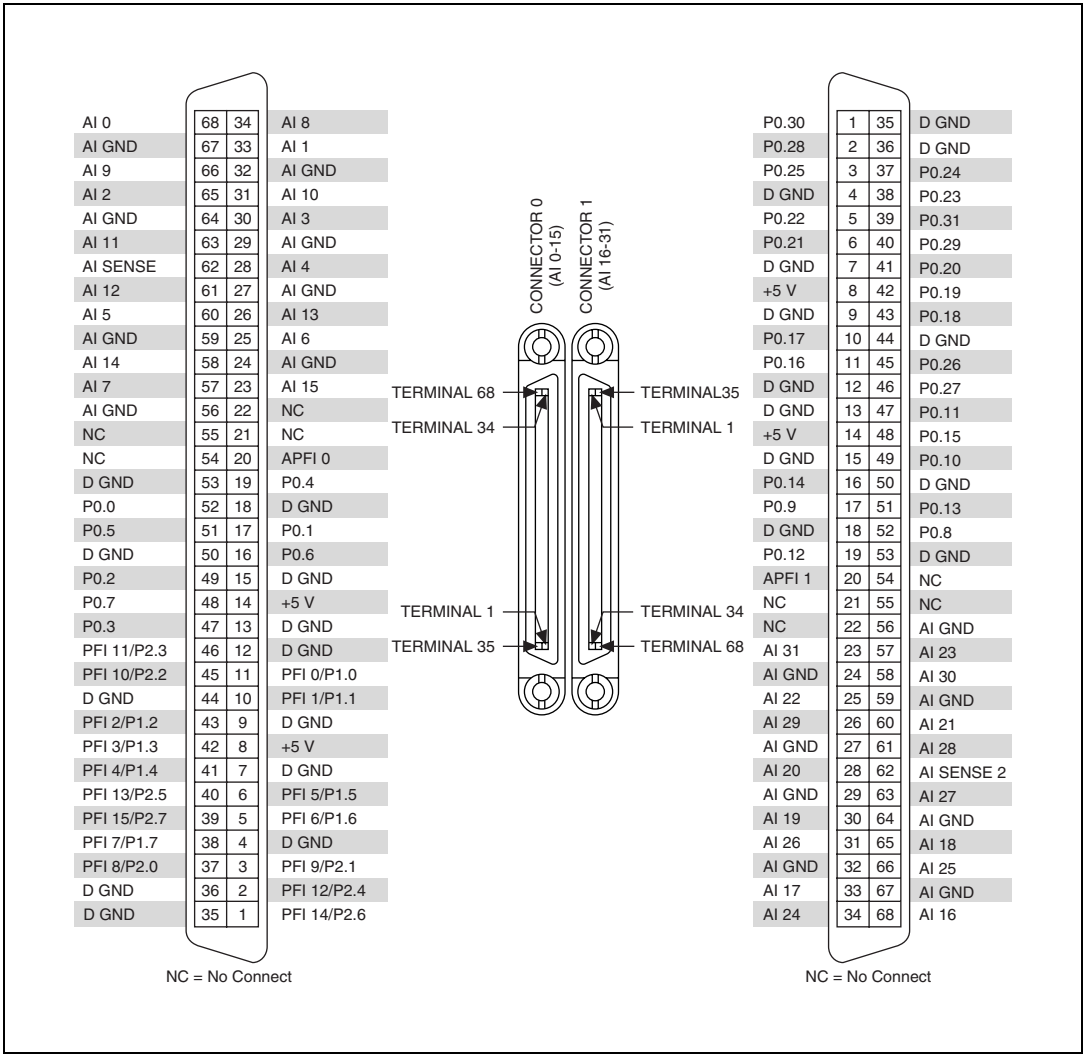

Figure 3. NI 6254 Pinout

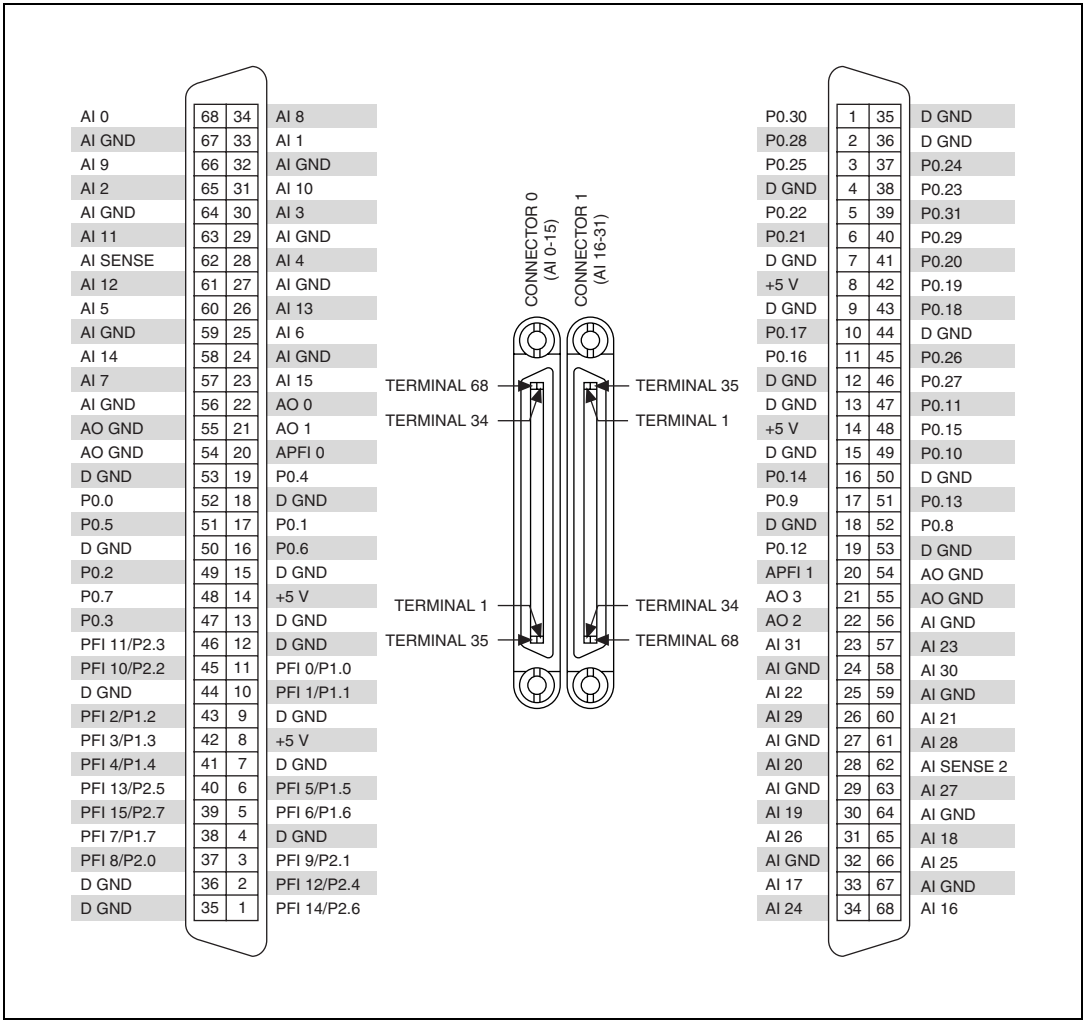

Figure 4. NI 6259 Pinout