PCIe-FIW Series
1394b PCI Express
Frame Grabber
User's Manual

Manual Rev. 2.03

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1 Introduction

The PCIe-FIW series are IEEE 1394b (FireWire 800) interface cards based on the PCI Express form factor and designed for high speed computer-based machine vision applications. This series consists of two main product families:

- PCIe-FIW62: two 1394b (FireWire 800) ports
- PCIe-FIW64: four 1394b (FireWire 800) ports

The PCIe-FIW series supports multiple 1394b device connections with data transfer rates up to 800 Mb/s, like most of the IEEE 1394b cameras. The IEEE 1394b standard also supports a power over cable feature to reduce wiring.

The 4-pin ATX power connector on the PCIe-FIW series allows the 1394 cameras that are connected to draw power. The LEDs on the front panel of the PCIe-FIW series will illuminate when a PCIe-FIW card is connected to a 1394b camera, thus making it is easy to identify the channel connection status.

The PCIe-FIW64 provides four isolated digital inputs and outputs for connecting to external devices such as position sensors. The PCIe-FIW64 also includes four isolated programmable trigger output pulses to manage trigger events such as activating a strobe light.

1.1 Features

- PCI Express compliant
  - PCIe-FIW62: x1 PCI Express
  - PCIe-FIW64: x4 PCI Express
- High-speed image transfer rates up to 800 Mb/s
- Provides industrial screw lock connector
- Status LED for channel activation
- Four isolated digital inputs/outputs
- Four isolated TTL level programmable trigger output pulses
- Supports Windows XP/XP Embedded/Vista

1.2 Applications

- Machine vision inspection systems
- Scientific research instrumentation
- Medical research instrumentation

2 Hardware Reference

2.1 PCIe-FIW64

2.1.1 PCIe-FIW64 Specifications

IEEE1394b Port

- Four IEEE1394b fully compliant cable ports at 100 Mb/s, 200 Mb/s, 400 Mb/s, and 800 Mb/s.
- Fully supports the IEEE P1394b-2002 standard.
- Fully compliant with the IEEE 1394-1995 standard for a high performance serial bus and the IEEE 1394a-2000 standard.
- Fully compliant with the 1394 Open Host Controller Interface Specification, Revision 1.1 and revision 1.2 draft.

Digital I/O and Trigger I/O Functions

- Four isolated digital inputs
- Four isolated digital outputs
- Four isolated trigger inputs
- Four isolated trigger outputs

Isolated Voltage

- Rated isolation voltage: 1000 V @ 60 seconds

Form Factor

- x4 PCI-express interface (compliant with the PCI
- Express Base Specification, Revision 1.1))

Dimensions

- W x L: 129.5 x 111.15 mm

Operating Environment

- Temperature: 0 to 55°C
- Humidity: 5 to 90% RHNC

Storage Environment

- Temperature: 0 to 85°C
- Humidity: 0 to 95% RHNC

Power Requirements

- ▷ PCIe-FIW64: +12 V max 200 mA, +3.3 V max 2.5 A

2.1.2 PCIe-FIW64 Outline

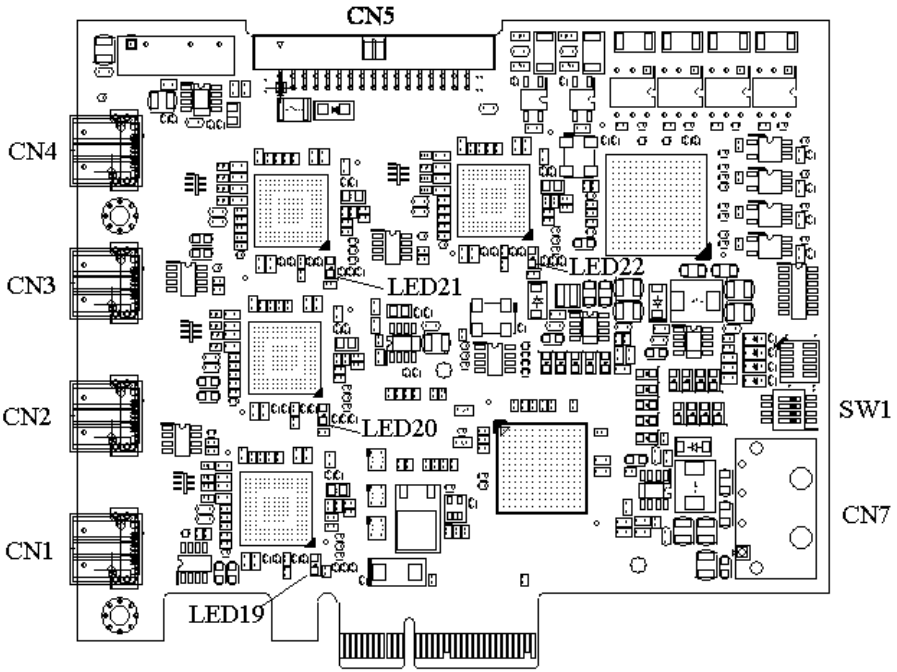
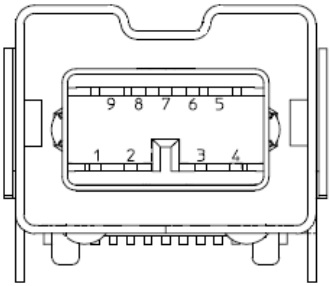


Figure 2-1: PCIe-FIW64 Outline

2.1.3 PCIe-FIW64 Connectors and Pin Definitions

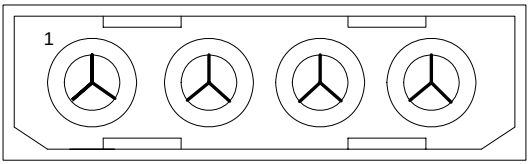
CN1-CN4: IEEE1394b Port



Pin	Signal	Pin	Signal
1	TPB-	6	VG
2	TPB+	7	SC
3	TPA-	8	VP
4	TPA+	9	TPB(R)
5	TPA(R)		

Table 2-1: 1394b Pinout

CN5: Additional 12 V Power Input Port



Pin	Signal
1	+12 V
2	GND
3	GND
4	NC

Table 2-2: Additional 12 V Power Input Port

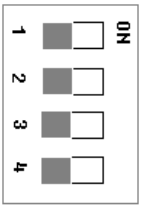
LED19-LED22: IEEE1394 Connection Status LEDs

Component	Function	Description
LED19	CN1 IEEE1394 bus connection status display.	Green light: Normal connection
LED20	CN2 IEEE1394 bus connection status display.	Green light: Normal connection
LED21	CN3 IEEE1394 bus connection status display.	Green light: Normal connection
LED22	CN4 IEEE1394 bus connection status display.	Green light: Normal connection

Table 2-3: IEEE1394 Connection Status LEDs

SW1: Card ID Select

Card ID: Maximum of four cards supported.



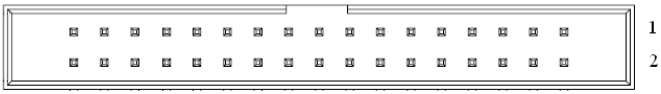
SW1		
Pin	**Signal Name**	**Default**
1	Board ID Select 0	ON
2	Board ID Select 1	ON
3	Non use	ON
4	Non use	ON

Table 2-4: Card ID Select

Card ID	Board ID Select 0	Board ID Select 1
0	ON	ON
1	OFF	ON
2	ON	OFF
3	OFF	OFF

Table 2-5: Card ID Select Table

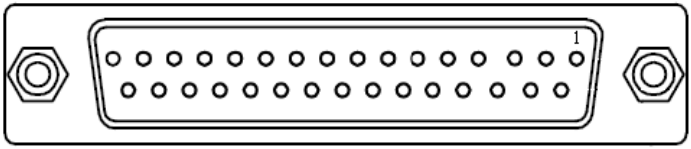
CN5: GPIO & Trigger



Pin	Pin Name	Type	Pin	Pin Name	Type
1	System Power(+12V)	OUT	2	System GND	
3	Digital input 1	IN	4	Digital input common 1	IN
5	Digital input 2	IN	6	Digital input common 2	IN
7	Digital input 3	IN	8	Digital input common 3	IN
9	Digital input 4	IN	10	Digital input common 4	IN
11	Digital output 1	OUT	12	Digital output common 1	OUT
13	Digital output 2	OUT	14	Digital output common 2	OUT
15	Digital output 3	OUT	16	Digital output common 3	OUT
17	Digital output 4	OUT	18	Digital output common 4	OUT
19	Trigger input 1	IN	20	Trigger input common 1	IN
21	Trigger input 2	IN	22	Trigger input common 2	IN
23	Trigger input 3	IN	24	Trigger input common 3	IN
25	Trigger input 4	IN	26	Trigger input common 4	IN
27	Trigger output 1	OUT	28	Trigger output 2	OUT
29	Trigger output 3	OUT	30	Trigger output 4	OUT
31	Frame GND		32	Frame GND	
33	Frame GND		34	Frame GND	

Table 2-6: GPIO & Trigger

Extension D-sub 37 Pin Cable Connector:



Pin	Pin Name	Type	Pin	Pin Name	Type
1	System Power(+12V)	OUT	20	System GND	
2	Digital input 1	IN	21	Digital input common 1	IN
3	Digital input 2	IN	22	Digital input common 2	IN
4	Digital input 3	IN	23	Digital input common 3	IN
5	Digital input 4	IN	24	Digital input common 4	IN
6	Digital output 1	OUT	25	Digital output common 1	OUT
7	Digital output 2	OUT	26	Digital output common 2	OUT
8	Digital output 3	OUT	27	Digital output common 3	OUT
9	Digital output 4	OUT	28	Digital output common 4	OUT
10	Trigger input 1	IN	29	Trigger input common 1	IN
11	Trigger input 2	IN	30	Trigger input common 2	IN
12	Trigger input 3	IN	31	Trigger input common 3	IN
13	Trigger input 4	IN	32	Trigger input common 4	IN
14	Trigger output 1	OUT	33	Trigger output 2	OUT
15	Trigger output 3	OUT	34	Trigger output 4	OUT
16	Frame GND		35	Frame GND	
17	Frame GND		36	Frame GND	
18	NC		37	NC	
19	NC				

Table 2-7: Extension Cable Connector

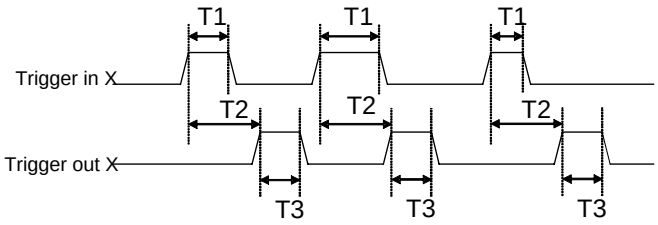
2.1.4 PCIe-FIW64 Trigger Delay Function

Trigger function description

The trigger function is based on the trigger output delay time, output signal pulse width, trigger signal level polarity, busy period and trigger input signal to produce a trigger output signal. The range of trigger delay setting is 0-1000 ms and one scale is 1 ms. The range of trigger output pulse width setting is 0.1-50 ms and one scale is 0.1 ms. The reference of trigger delay function depends on trigger input signal rising edge or falling edge. The polarity setting has four values:

- A value of “0” is for the trigger input signal falling edge and trigger output low active level signal.
- A value of “1” is for the trigger input signal falling edge and trigger output high active level signal.
- A value of “2” is for the trigger input signal rising edge and trigger output low active level signal.
- A value of “3” is for the trigger input signal rising edge and trigger output high active level signal.

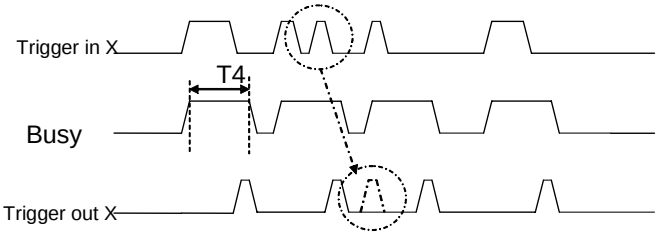
Trigger Control Timing Chart



Symbol	Characteristic	Specification
T1	Trigger input pulse width	0.1 msec (min.)
T2	Trigger delay	0 to 1000 msec selectable (1 msec step) Actual delay = Selected delay time
T3	Output trigger pulse width	0.1 to 50 msec selectable (0.1 msec step)

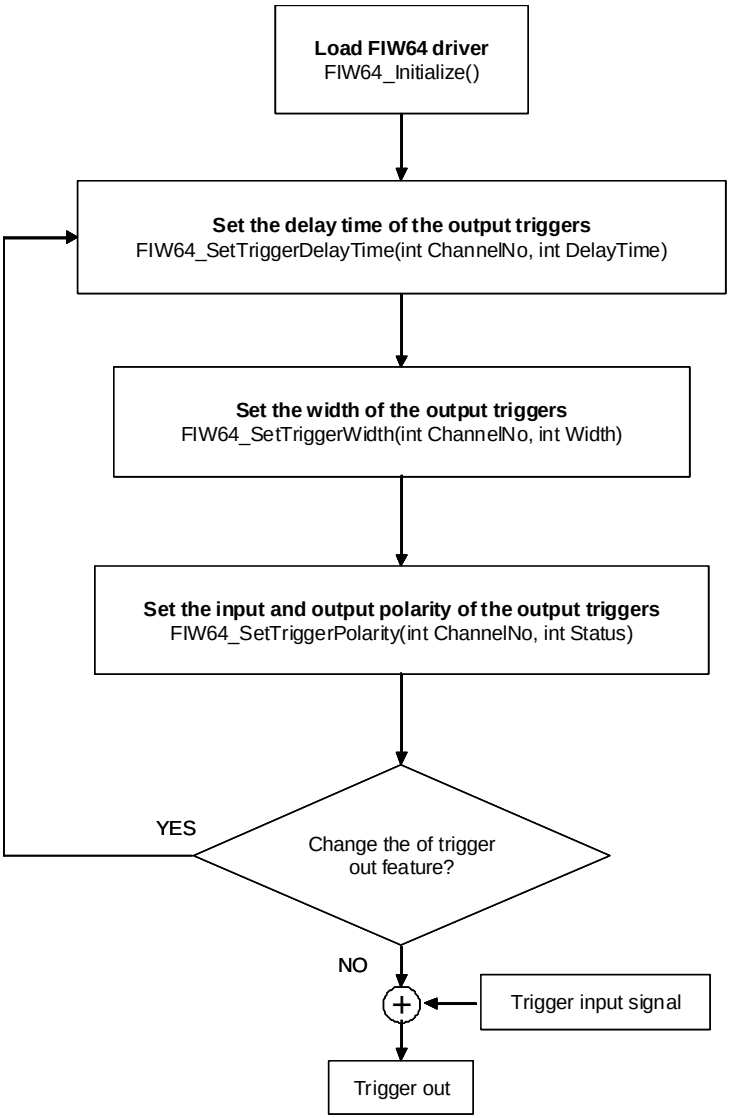
Table 2-8: Trigger Control Timing

Trigger Busy Control



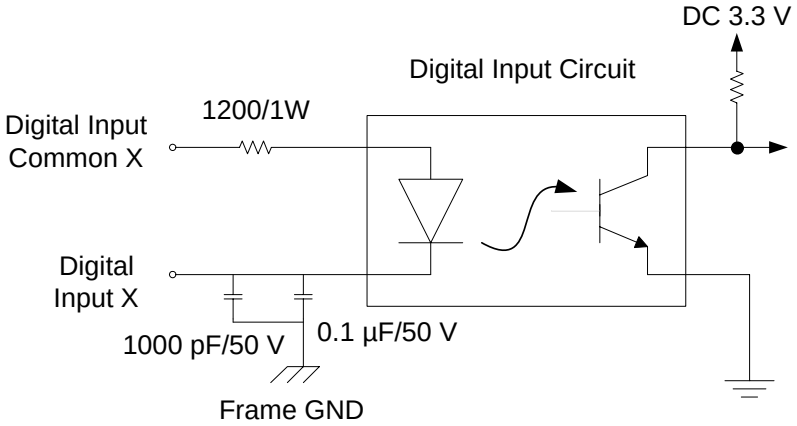
Symbol	Characteristic	Specification
T4	Trigger busy timer	T3 + 0.1 msec. The busy flag is set and the trigger busy timer starts counting when the Trigger In signal is detected. The Trigger Busy flag is reset when the trigger busy timer is done counting When the Trigger Busy flag is set, the Trigger In signal is ignored.

Trigger control setting flow chart

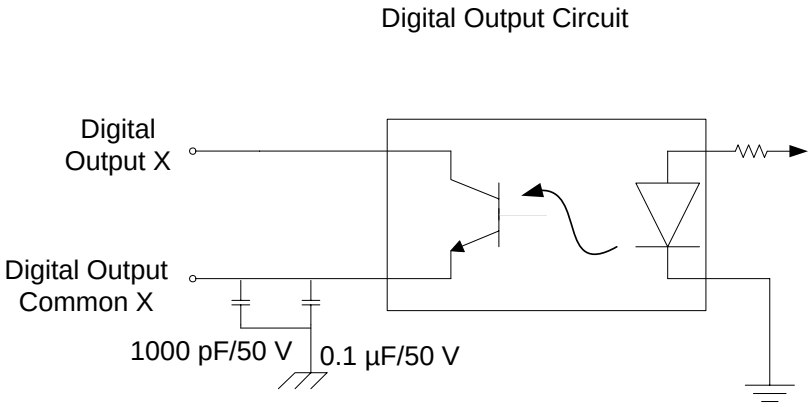


2.1.5 Input and Output Circuits Diagrams

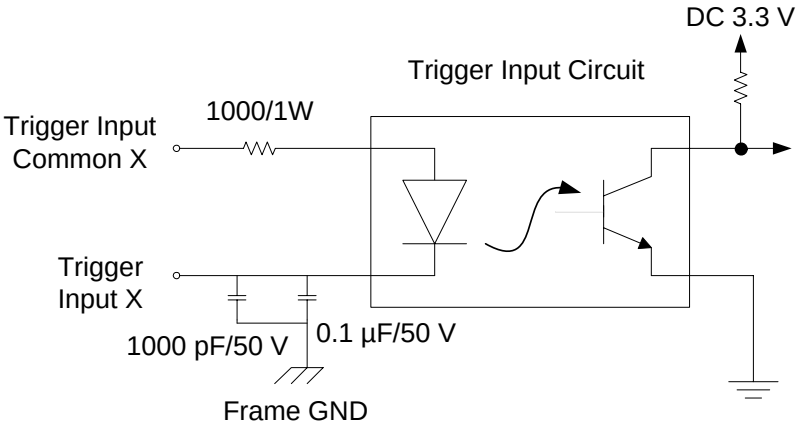
Digital Input Circuit



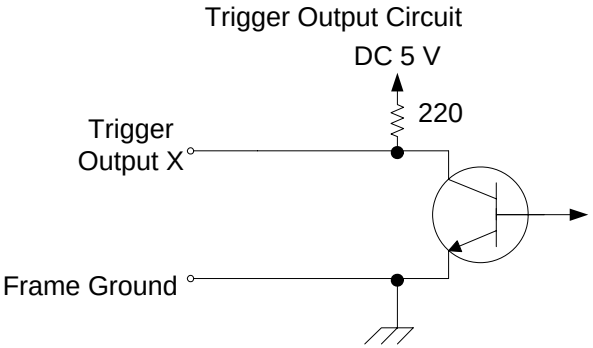
Digital Output Circuit



Trigger Input Circuit

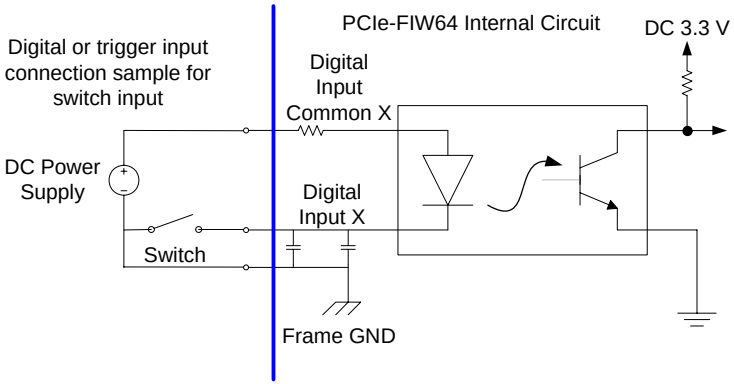


Trigger Output Circuit

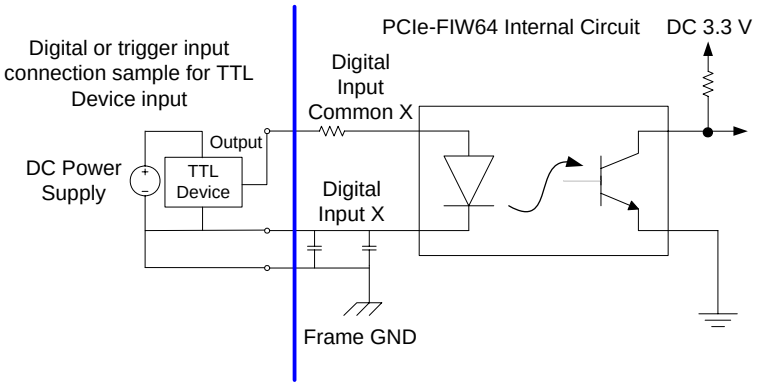


2.1.6 User Device I/O Connection Examples

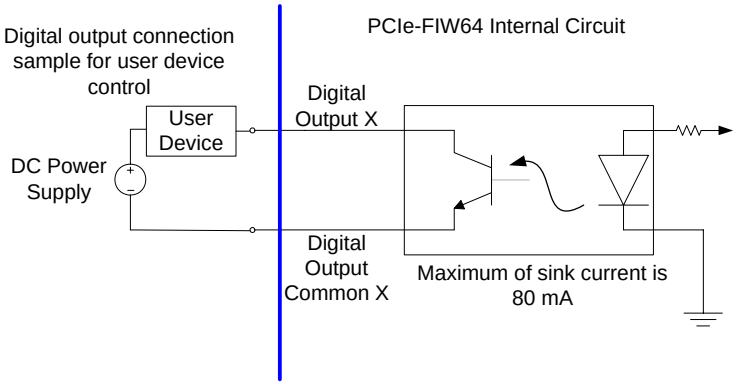
Digital input or trigger input connection for switch input.



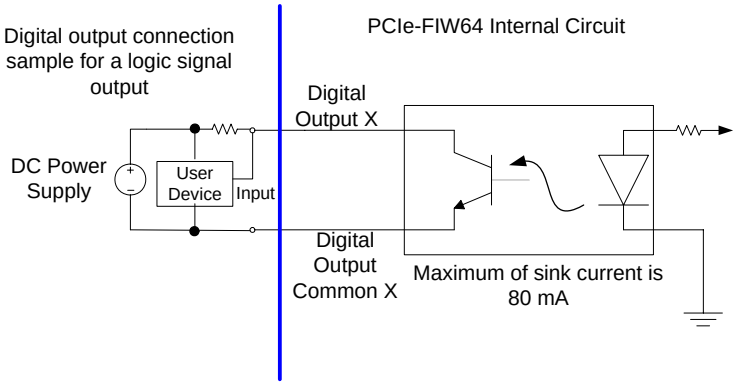
Digital input or trigger input connection for TTL signal input.
The response of the computer needs to be inverted in this connection condition mode. *If the external device output controls a digital input common con-tact, then the response from the computer needs to be inverted.



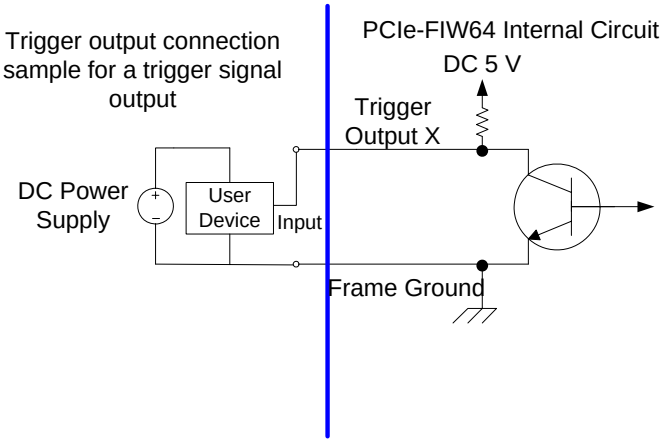
Digital output connection for user device control.



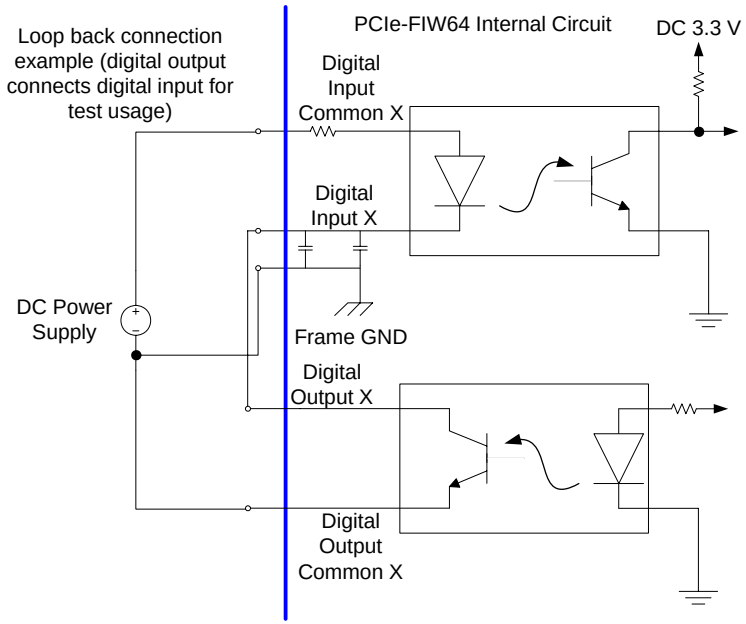
Digital output connection for a logic signal output.



Trigger output connection for a trigger signal output.



Loop back connection.



2.1.7 Hardware Features

Function	Electronic Specification
Isolated Digital Input	Photo Coupled Input x 4 ch
Input voltage range	0 to 25 V
Low level	0 to 0.5 V
High Level	2 to 25 V
Isolated Digital Output	Photo Coupled Output x 4 ch
Load voltage range	3 to 24 V
Output sink current	80 mA (Max)
Output voltage drop	1.0 V (Max)
Leak current	0.1 mA (Max)
Reverse voltage	-6 V
Isolated Trigger Input	Photo Coupled Trigger input x 4 ch
Input voltage range	0 to 25 V
Low level	0 to 0.5 V
High level	2.4 to 25 V
Polarity	Positive / Negative Selectable
Minimum pulse width	0.1 msec
Isolated Trigger out	Photo Coupled Trigger output x 4 ch
Load voltage range	0 to 5 V
Output sink current	40 mA (Max)
Output voltage drop	0.4 V Max (@16 mA)
Trigger Out Control	
Trigger delay	0 msec to 1000 msec selectable (1 msec step.)
Trigger out pulse width	0.1 msec to 50 msec selectable (0.1 msec step)
Polarity	Positive / Negative Selectable

Table 2-9: Specifications

2.2 PCIe-FIW62 Specifications

External device signal input

- ▷ Channel ports (1 and 2) : 1394b 9-pin connector with screw
- ▷ 1394b differential signals

Form factor

- ▷ PCI-express x1 interface

User EEPROM

- ▷ Includes 2 kbit available EEPROM

Dimension

- ▷ W x L: 78.6 mm x 105.7 5mm

Power Requirements

- ▷ +3.3 V, max 0.22 A

2.2.1 PCIe-FIW62 Appearance

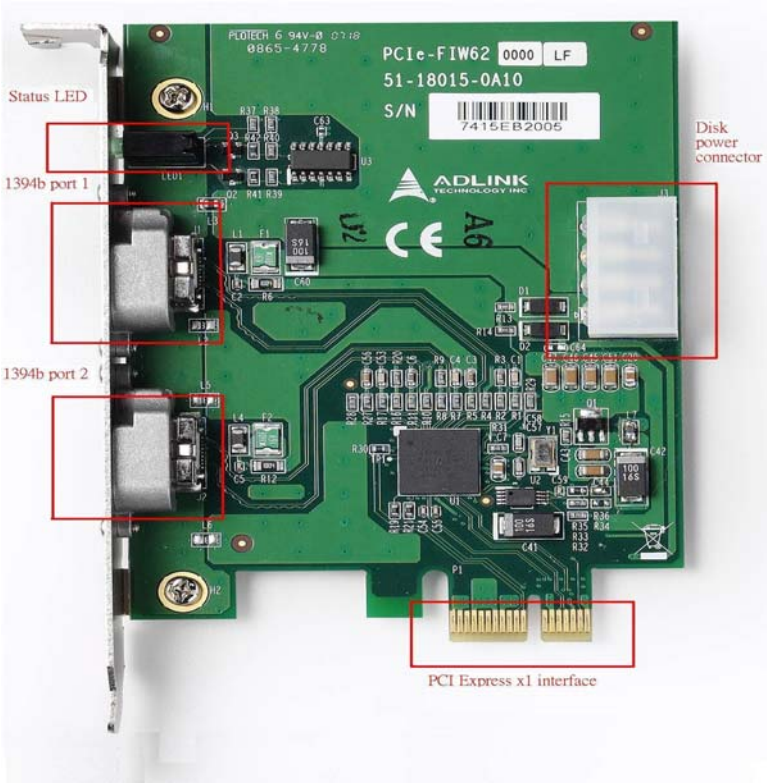
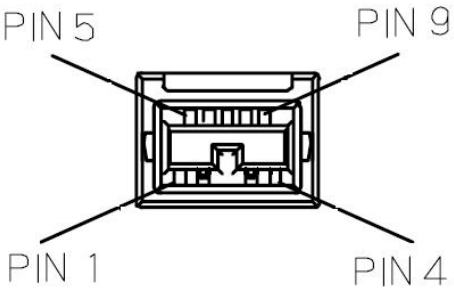


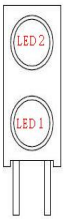
Figure 2-2: PCIe-FIW62 Diagram

2.2.2 PCIe-FIW62 Connectors and Pin Definitions



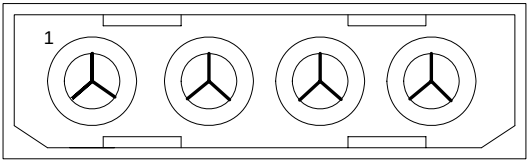
Pin Number	Pin Definition	Function
1	TPB-	Twisted Pair B, Minus
2	TPB+	Twisted Pair B, Plus
3	TPA-	Twisted Pair A, Minus
4	TPA+	Twisted Pair A, Plus
5	TPA (R)	Ground, Twisted Pair A
6	VG	Power Ground
7	NC	No Connection
8	VP	Power Voltage
9	TPB (R)	Ground, Twisted Pair B

Table 2-10: 1394b Pinout



LED No.	Function
LED 1	Port 1 active
LED 2	Port 2 active

Table 2-11: Status LED



Pin	Signal
1	+12 V
2	GND
3	GND
4	NC

Table 2-12: Disk Power Pinout

3 Installation Guide

3.1 Hardware Installation

Use the following steps to install the PCIe-FIW series card on the PCI Express bus:

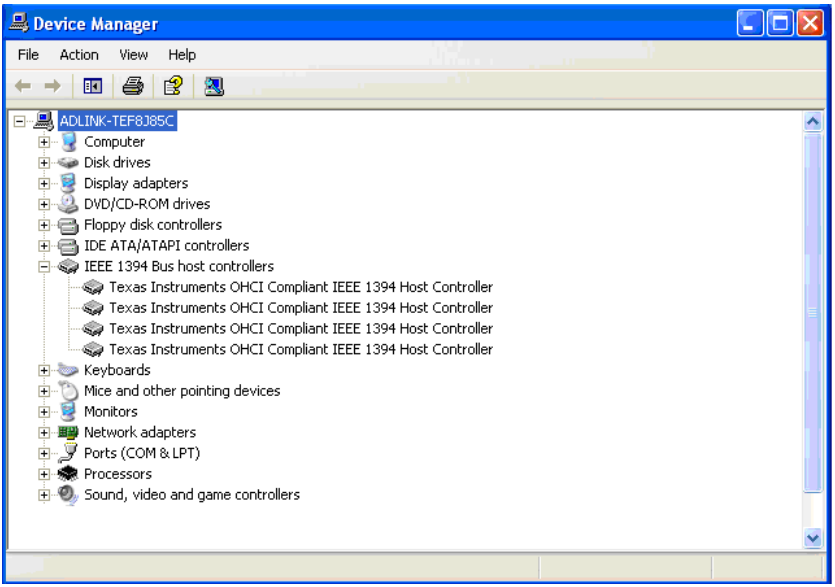
1. Remove the computer cover using the instructions from the computer manual.
2. Check that there is an empty PCI express slot accommodated the board. If there is no empty slot, remove a PCI Express board from the computer to make room for the PCIe-FIW series card and take note of the chosen slot number.
3. Remove the blank metal plate located at the back of the selected slot (if any). Keep the removed screw to fasten the PCIe-FIW series card after installation.
4. Carefully position the PCIe-FIW series card in the selected PCI Express slot. If using a tower computer, align the board with the board slots.
5. Press the card in firmly, but carefully into the connector.
6. Anchor the board by replacing the screw.
7. Connect the device via the 1394 connector.
8. Turn on the computer.

Note: The PCIe-FIW64 can be installed in a PCI Express x4, x8, x16 slot, and the PCIe-FIW62 can be installed in a PCI express x1, x4, x8, Xx16 slot

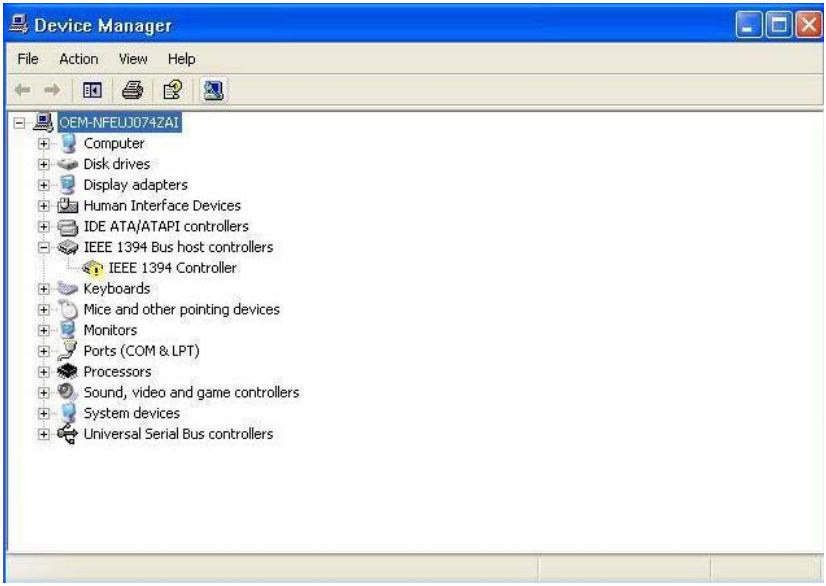
3.2 Driver Installation

1. Microsoft Windows will automatically install 1394 driver through a built-in OHCI IEEE-1394 driver.
2. Go to the **Device Manager** and check **IEEE 1394 Bus host controllers**, you should see the following item:

   ▷ **Texas Instruments OHCI Compliant IEEE 1394 Host Controller**

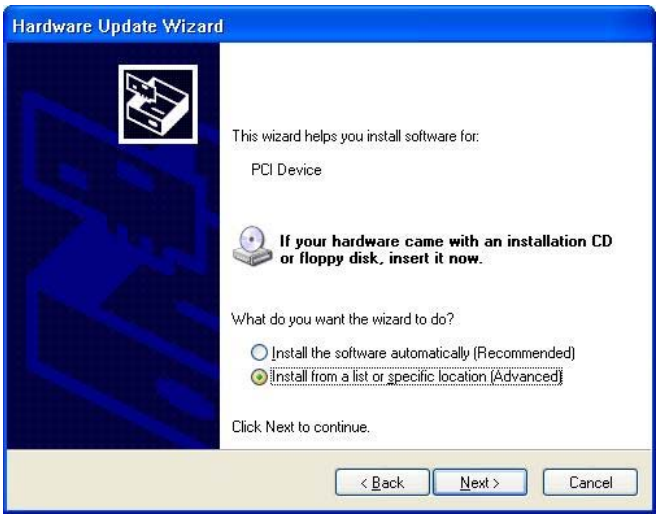


2.1. If there is a yellow exclamation mark in front of the new driver name, you will need to setup the driver manually.

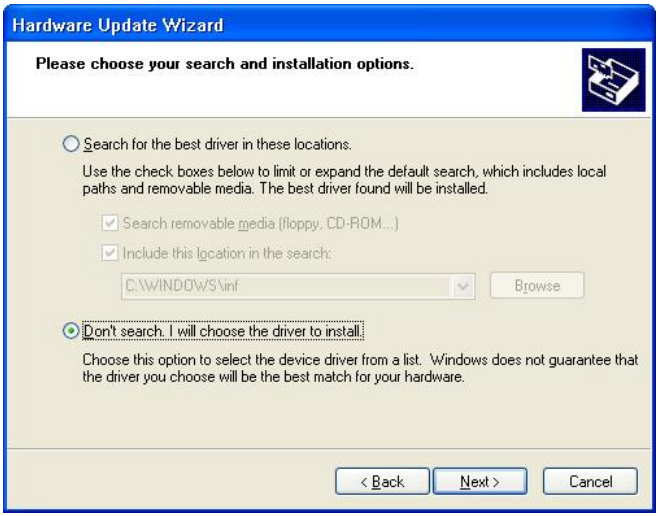


2.2. Right-click **IEEE 1394 Controller** and select **Update driver**.

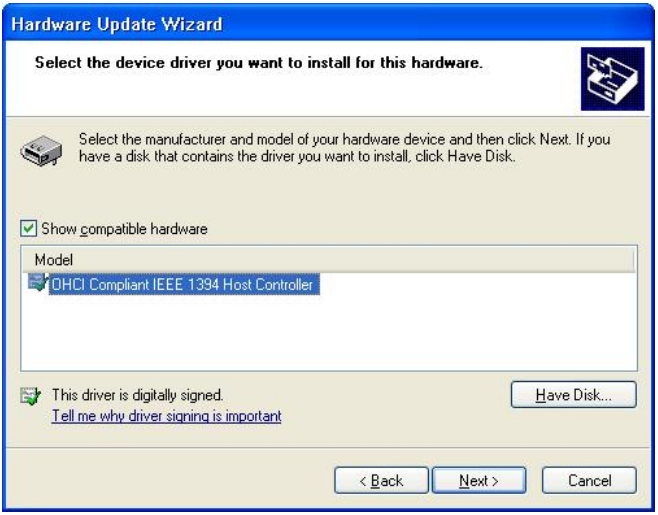
2.3. Click **Next**

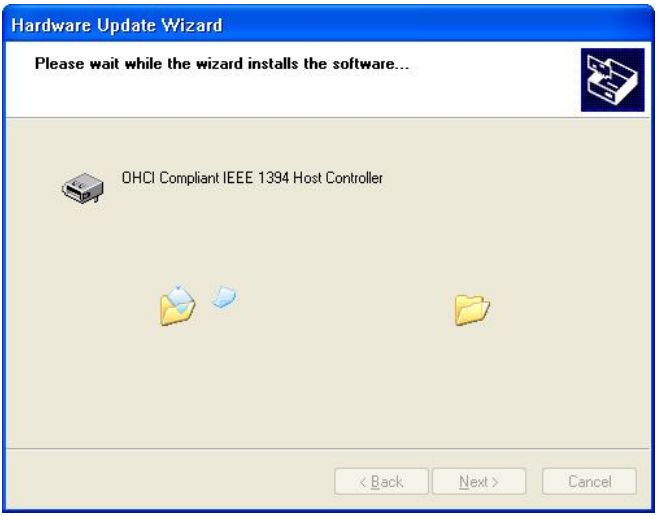


2.4. Click **Next**



2.5. Click **Next**

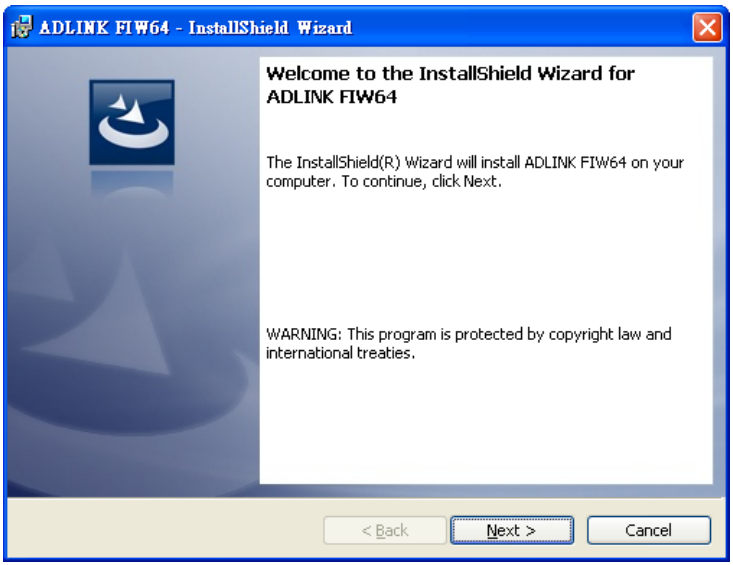




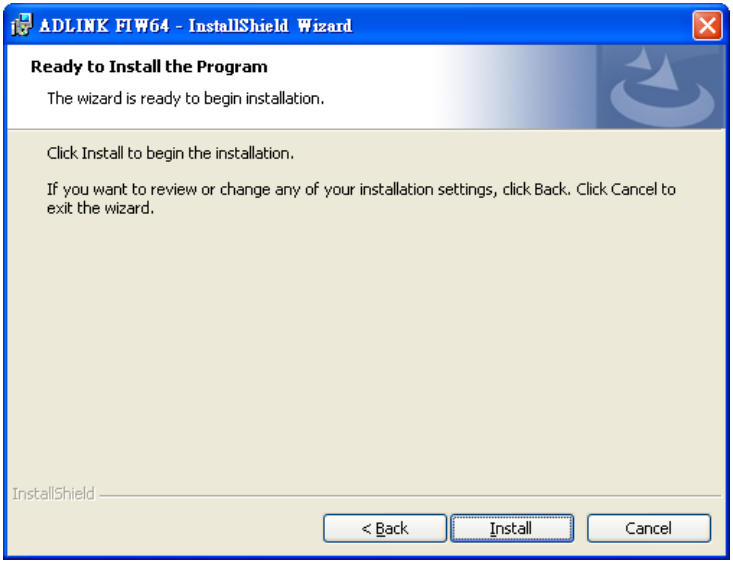
2.6. Click **Finish** to complete the wizard.

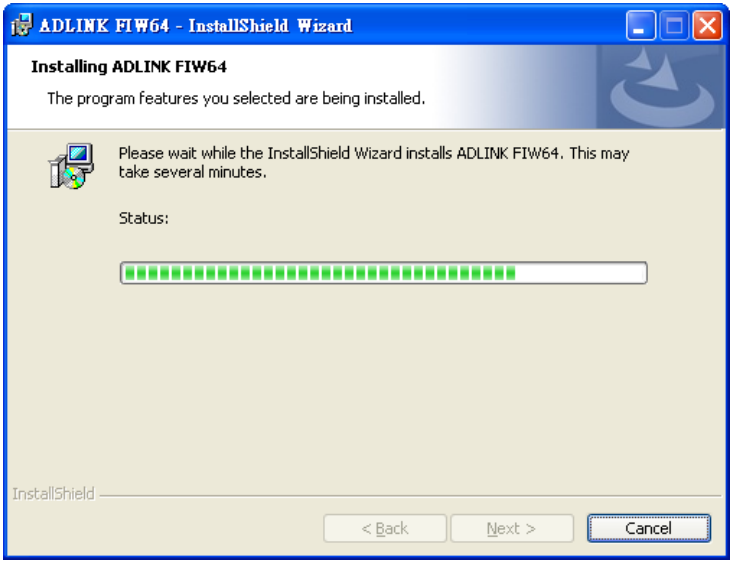
3. For the PCIe-FIW64, after installing the IEEE-1394 driver, please double-click **FIW64_SetupDisk.exe** to start driver installation of the ADLINK FIW64 DI/O and trigger function.

4. Click **Next** to continue driver installation.

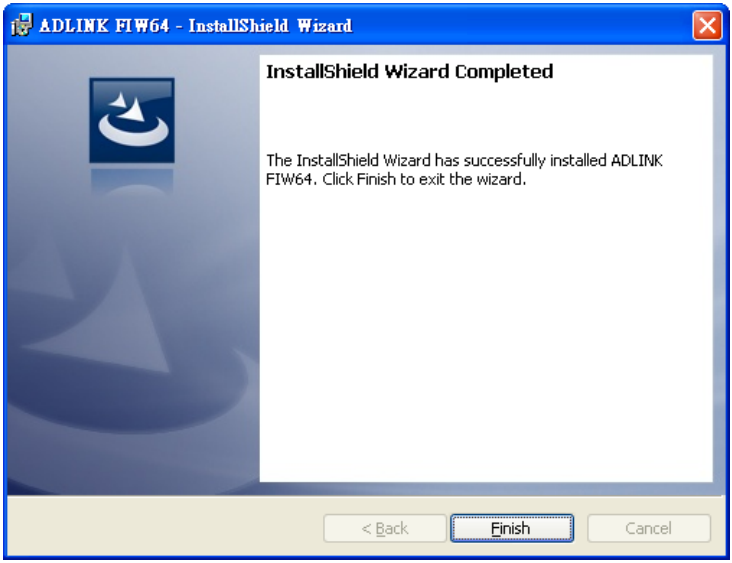


5. Click **Install** to begin the installation.





6. Click **Finish** to complete driver installation.



Note: If using Windows Vista, there is an important setting must be performed in order for the PCIe-FIW series to function properly. Perform the following to turn off the User Account Control (UAC).

1. Click **Start** -> **Settings** -> **Control Panel** -> **User Accounts** -> **Turn User Account Control On or Off**.
2. Uncheck **Use User Account Control (UAC) to help protect your computer**.
3. Click **OK**.
4. Restart the computer and the PCIe-FIW series card will work normally.

4 Function Library

4.1 Function List

Function Name	Description
System Functions	
FIW64_Initialize	Loads the FIW64 driver. This function must be called before any other functions.
FIW64_GetTotalDeviceNum	Obtain the number of the FIW64 cards in the system.
FIW64_GetTotalDeviceID	Obtain the CardIDs of the FIW64 cards in the system.
FIW64_ResetDevice	Resets the FIW64 card to the default status.
FIW64_GetFirmwareVersion	Obtain the firmware version of the FIW64 card.
FIW64_GetErrorMessage	Obtain the Error Message by returning the value of functions.
DIO Functions	
FIW64_SetDO	Set the general purpose digital output status.
FIW64_GetDI	Obtain the general purpose digital input status.
Trigger Functions	
FIW64_SetTriggerDelayTime	Set the delay time of the output triggers.
FIW64_GetTriggerDelayTime	Obtain the delay time of the output triggers.
FIW64_SetTriggerWidth	Set the width of the output triggers.
FIW64_GetTriggerWidth	Obtain the width of the output triggers.
FIW64_SetTriggerPolarity	Set the input and output polarity of the output triggers.
FIW64_GetTriggerPolarity	Obtain the input and output polarity of the output triggers.

4.2 Functions

4.2.1 FIW64_Initialize

Description

Loads the FIW64 driver. This function must be called before any other functions.

Syntax

```
int FIW64_Initialize();
```

4.2.2 FIW64_GetTotalDeviceNum

Description

Obtain the number of the FIW64 cards in the system.

Syntax

```
int FIW64_GetTotalDeviceNum(int *DeviceNum);
```

Parameters

`DeviceNum`

[out] Pointer to a 32-bit integer which stores the read out Card Number.

4.2.3 FIW64_GetTotalDeviceID

Description

Obtain the CardIDs of the FIW64 cards in the system.

Syntax

```
int FIW64_GetTotalDeviceID(int *DeviceID, int
ArrayLen );
```

Parameters

`DeviceID`

[out] Pointer to a 32-bit integer array which stores the read out CardID(s) defined by the DIP switch on FIW64.

`ArrayLen`

[in] Length of the 32-bit integer array of DeviceID.

4.2.4 FIW64_ResetDevice

Description

Resets the FIW64 card to the default status.

Syntax

```
int FIW64_ResetDevice(int ChannelNo);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

If ChannelNo is set to -1, all channels will be reset.

4.2.5 FIW64_GetFirmwareVersion

Description

Obtain the firmware version of the FIW64 card.

Syntax

```
int FIW64_GetFirmwareVersion(int ChannelNo, int
*Version);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`Version`

[out] Pointer to a 32-bit integer variable which stores the read out firmware version.

4.2.6 FIW64_SetDO

Description

Set the general purpose digital output status.

Syntax

```
int FIW64_SetDO(int ChannelNo,int Status);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`Status`

[in] A 32-bit integer variable which represents the status of digital output.

0: Low

1: High

4.2.7 FIW64_GetDI

Description

Obtain the general purpose digital input status.

Syntax

```
int FIW64_GetDI(int ChannelNo,int *Status);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`Status`

[out] Pointer to a 32-bit integer variable which stores the read out digital input status.

4.2.8 FIW64_GetTriggerDelayTime

Description

Obtain the delay time of the output triggers.

Syntax

```
int FIW64_GetTriggerDelayTime(int ChannelNo,int
*DelayTime);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`DelayTime`

[out] Pointer to a 32-bit integer variable which stores the read out delay time of output triggers.

4.2.9 FIW64_SetTriggerDelayTime

Description

Set the delay time of the output triggers.

Syntax

```
int FIW64_SetTriggerDelayTime(int ChannelNo,int
DelayTime);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`DelayTime`

[in] A 32-bit integer variable which specifies the delay time of output triggers.

The value should be 0 - 1000 (units: 1 ms).

4.2.10 FIW64_GetTriggerWidth

Description

Obtain the width of the output triggers.

Syntax

```
int FIW64_GetTriggerWidth(int ChannelNo,int *
Width);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`Width`

[out] Pointer to a 32-bit integer variable which stores the read out width of output triggers.

4.2.11 FIW64_SetTriggerWidth

Description

Set the width of the output triggers.

Syntax

```
int FIW64_SetTriggerWidth(int ChannelNo,int Width);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. ccan be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`Width`

[in] A 32-bit integer variable which specifies the width of output triggers.

The value should be 0 - 500 (units: 0.1 ms).

4.2.12 FIW64_GetTriggerPolarity

Description

Obtain the polarity of the input and output triggers.

Syntax

```
int FIW64_GetTriggerPolarity(int ChannelNo,int
*Status);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`Status`

[out] Pointer to a 32-bit integer variable which stores the read out polarity of the input and output triggers.

0: meaning low input polarity and low output polarity

1: meaning low input polarity and high output polarity

2: meaning high input polarity and low output polarity

3: meaning high input polarity and high output polarity

4.2.13 FIW64_SetTriggerPolarity

Description

Set the input and output polarity of the output triggers.

Syntax

```
int FIW64_SetTriggerPolarity(int ChannelNo,int
Status);
```

Parameters

`ChannelNo`

[in] Channel No. of the FIW64 card. The channel No. can be 0, 1, 2 and 3 in the device whose Card ID is 0; moreover, it can be 4, 5, 6 and 7 in the device whose Card ID is 1, etc.

`Status`

[in] A 32-bit integer variable which specifies the polarity of the input and output triggers.

The value will be 0 for low input polarity and low output polarity.

The value will be 1 for low input polarity and high output polarity.

The value will be 2 for high input polarity and low output polarity.

The value will be 3 for high input polarity and high output polarity.

4.2.14 FIW64_GetErrorMessage

Description

Obtain the Error Message by returning the value of functions.

Syntax

```
int FIW64_GetErrorMessage(int ErrorCode, char*
ErrorMessage);
```

Parameters

`ErrorCode`

[in] A 32-bit integer variable which specifies the error code.

`ErrorMessage`

[out] Pointer to a character array which stores the read out error message.

4.3 Error Codes

Error Code	Meaning
0	ERROR_NoError
-1	ERROR_DeviceNotExist
-2	ERROR_LoadDriverFail
-3	ERROR_DeviceCannotOpen
-4	ERROR_DeviceCannotAccess
-5	ERROR_Invalid_ChannelNo
-6	ERROR_SPIFunctionError
-7	ERROR_ParameterExceedLimit
-8	ERROR_CardIDError