PXIe-9852

2-CH 14-Bit 200 MS/s Digitizer

User's Manual

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Revision History

Revision	Release Date	Description of Change(s)
2.00	12/29/2013	Initial Release

Preface

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Disclaimer

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ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE:

Additional information, aids, and tips that help users perform tasks.

CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The PXIe-9852 is a high-speed 2-CH 14-Bit 200 MS/s digitizer, specifically designed for applications such as LIDAR testing, optical fiber testing and radar signal acquisition. Analog input with 90 MHz bandwidth receives ±10V high speed signals with 50Ω impedance, and a simplified front-end design and highly stable onboard reference provide both highly accurate measurement results and high dynamic performance.

Ideal for environments requiring real-time acquisition and transfer of data, the PXIe-9852 is based on the PCI Express Gen 2 x4 bus as interface. When signals are converted from analog to digital, continual data transfer to host system memory is enabled by PCI Express high bandwidth capability.

The PXIe-9852 is auto-calibrated with an onboard reference circuit calibrating offset and acquiring analog input errors. Following auto-calibration, the calibration constant is stored in EEPROM, such that these values can be loaded and used as needed by the board. There is no requirement to calibrate the module manually.

1.1 Features

- PXI Express specification Rev. 1.0 compliant
- Up to 200 MS/s sampling rate
- 2 simultaneous analog inputs
- High resolution 14-Bit ADC
- Up to 90 MHz bandwidth for analog input
- One GB onboard storage memory
- Scatter-Gather DMA data transfer for high-speed data streaming
- Supports signal averaging
- Support for:
  - one external digital trigger input
  - one digital trigger output to external instrument
  - one external clock input
  - auto-calibration

1.2 Applications

- Distributed Temperature Sensing (DTS)
- Video IC testing
- Physics laboratory and research environments
- Cable fault location and partial discharge monitoring for power applications

1.3 Specifications

1.3.1 Analog Input

Channel Characteristics		Comment
Channels	2 single-ended	
Connector type	SMA	
Input coupling	AC or DC, software selectable	
AC coupling cutoff frequency	11 Hz	
ADC resolution	14-Bit	
Input signal range	±0.2V, ±2V or ±10V	
Bandwidth (-3dB)	90 MHz	
Overvoltage	±10V	1MΩ
	±10V sinewave / 7Vrms with |Peaks| < 10V	50Ω
Input impedance	50Ω or 1MΩ, software selectable	
Offset error	±1 mV	
Gain error	±0.65%	
SNR	56dB	1MΩ, ±0.2V
	62dB	1MΩ, ±2V
	62dB	1MΩ, ±10V
	60dB	50Ω, ±0.2V
	62dB	50Ω, ±2V

Channel Characteristics		Comment
THD	-73dB	1MΩ, ±0.2V
	-69dB	1MΩ, ±2V
	-65dB	1MΩ, ±10V
	-73dB	50Ω, ±0.2V
	-69dB	50Ω, ±2V
SFDR	72dB	1MΩ, ±0.2V
	72dB	1MΩ, ±2V
	72dB	1MΩ, ±10V
	68dB	50Ω, ±0.2V
	68dB	50Ω, ±2V
CrossTalk	-80dB	±0.2V, ±2V

CAUTION: While ±10V, 50Ω acquisition is available, overvoltage protection only applies to 7Vrms. Any ±10V sine wave with an offset or DC voltage over ±7V input can cause damage.

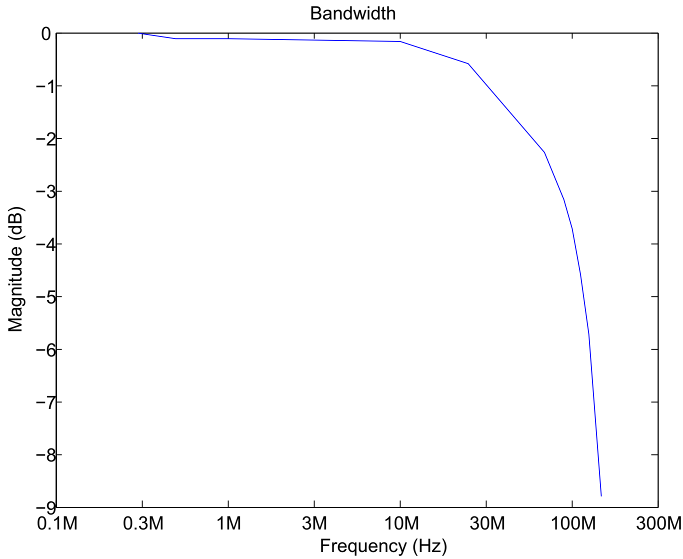

Figure 1-1: Analog Input Channel Bandwidth, ±0.2 Vpp

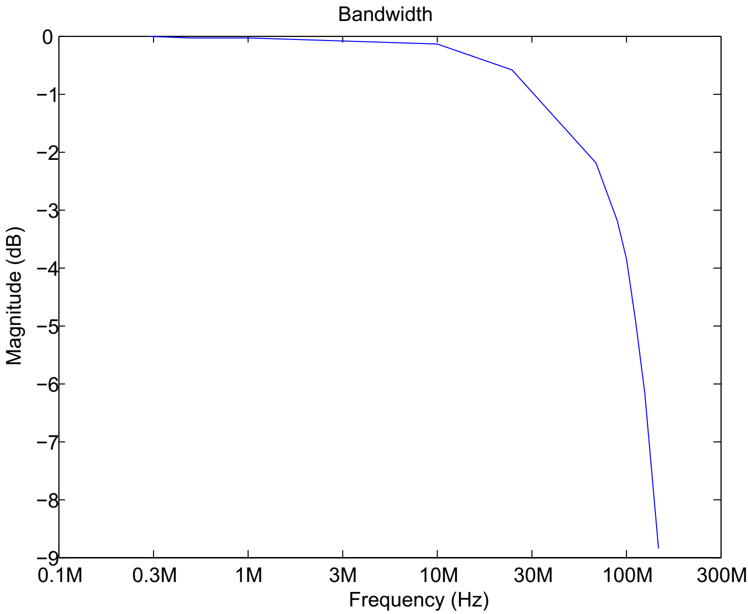

Figure 1-2: Analog Input Channel Bandwidth, ±2 Vpp

1.3.2 Timebase

Sample Clock		Comment
Timebase options	Internal : on board synthesizer	
	External : CLK IN (front panel), PXI_CLK10, and PXIe_CLK100	
Sampling clock frequency	Internal : 200MHz	3.052kS/s to 200MS/s
	External : 40MHz ~ 200MHz (CLK IN)	
Timebase accuracy	< ± 25ppm	
External reference clock source	Front panel, PXI_CLK10, and PXIe_CLK100	

Sample Clock		Comment
External reference clock	10MHz	
External reference clock input range	500mVpp ~ 5Vpp	AC / DC compliant, 50Ω load impedance
External sampling clock input range	1Vpp ~ 5Vpp	AC / DC compliant, 50Ω load impedance

Table 1-1: Timebase

1.3.3 Triggers

Trigger Source & Mode	
Trigger source	Software, external digital trigger, analog trigger, PXI_STAR, PXI_trigger bus [0..7], and PXIe_DSTARB
Trigger mode	Post trigger, delay trigger, pre-trigger, or middle trigger, re-trigger for post trigger and delay trigger modes

Table 1-2: Trigger Source & Mode

Digital Trigger Input	
Sources	Front panel SMA connector
Compatibility	3.3 V TTL, 5 V tolerant
Input high threshold	2.0 V
Input low threshold (VIL)	0.8 V
Maximum input overload	-0.5 V ~ +5.5 V
Trigger polarity	Rising or falling edge
Pulse width	20 ns minimum

Table 1-3: Digital Trigger Input

Digital Trigger Output	
Compatibility	5 V TTL
Output high threshold (VOH)	2.4 V
Output low threshold (VOL)	0.2 V
Trigger polarity	Positive or negative
Pulse width	50 ns, 100 ns, 150 ns, 200 ns, 500 ns, 1 μs, 2 μs, 7.5 μs, and 10 μs
Trigger output driving capacity	Capable of driving 50Ω load

Table 1-4: Digital Trigger Output

1.3.4 General Specifications

Specifications	
Physical dimensions	160 (W) x 100 (H) mm (6.24 x 3.9 in.)
Bus	
Bus interface	PCI Express Gen 2 x 4
Environmental Tolerance	
Operating	Temperature: 0°C - 55°C Relative humidity: 5% - 95%, non-condensing
Storage	Temperature: -20°C - +80°C Relative humidity: 5% - 95%, non-condensing

Calibration	
Onboard reference	+5 V and +2.5 V
Temperature coefficient	3.0 ppm/°C
Warm-up time	15 minutes

Power Consumption		
Power Rail	**Standby Current (mA)**	**Full Load (mA)**
+3.3 V	766	782
12 V	882	970

1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW®.

All software options are included in the ADLINK All-in-One CD. Commercial software drivers are protected with licensing codes. Without the code, you may install and run the demo version for trial/demonstration purposes for only up to two hours. Contact your ADLINK dealer to purchase the software license.

1.4.1 SDK

For customers who want to write their own programs, ADLINK provides the following software development kits.

- DAQPilot for Windows, compatible with various application environments, such as VB.NET, VC.NET, VB/VC++, BCB, and Delphi
- DAQPilot for LabVIEW
- Toolbox adapter for MATLAB

1.4.2 WD-DASK

WD-DASK includes device drivers and DLL for Windows XP/7/8. DLL is binary compatible across Windows XP/7/8. This means all applications developed with WD-DASK are compatible with these Windows operating systems. The development environment may be VB, VB.NET, VC++, BCB, and Delphi, or any Windows programming language that allows calls to a DLL. The WD-DASK user and function reference manuals are on the ADLINK All-in-One CD.

1.5 Device Layout and I/O Array

NOTE: All dimensions are in mm

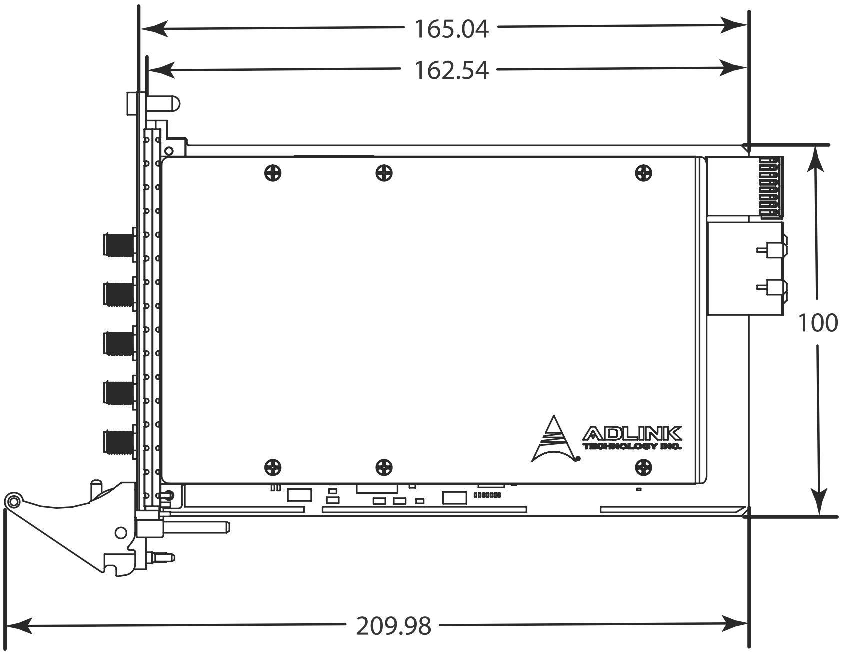

Figure 1-3: PXIe-9852 Schematic

The PXIe-9852 I/O array is labeled to indicate connectivity, as shown.

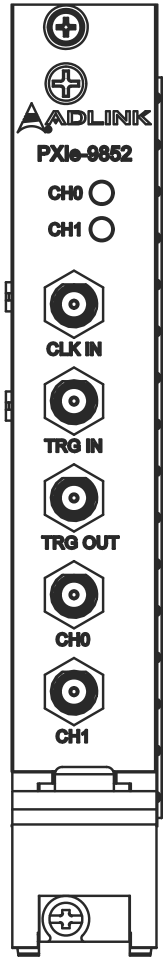

Figure 1-4: PXIe-9852 I/O Array

Name	Faceplate Legend	Type	Remark
CH0	N/A	Blue	On indicates CH0 acquisition ongoing Off indicates CH0 acquisition stopped
CH1	N/A	Blue	On indicates CH1 acquisition ongoing Off indicates CH1 acquisition stopped
Ext. Clock Input	CLK IN	SMA Screw	Input for external reference clock or sample clock to digitizer
Ext. Digital Trigger Input	TRG IN		External digital trigger input, receiving trigger signal from external instrument and initiating acquisition
Trigger Output	TRG OUT		Trigger output, in which every time acquisition begins, a pulse synchronized with Timebase clock asserts and is output through this connector, at pulse width programmable from 50ns to 10μs via software
Analog Input	CH0		Analog input channel
Analog Input	CH1		Analog input channel

Table 1-5: PXIe-9852 I/O Array Legend

2 Getting Started

This chapter describes proper installation environment, installation procedures, package contents and basic information users should be aware of regarding the PXIe-9852.

NOTE:

Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

2.1 Installation Environment

When unpacking and preparing to install, please refer to Important Safety Instructions.

Only install equipment in well-lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Antistatic mat

ADLINK PXIe-9852 DAQ modules are electrostatically sensitive and can be easily damaged by static electricity. The module must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the carton and packaging for damage. Shipping and handling could cause damage to the equipment inside. Make sure that the equipment and its associated components have no damage before installation.

CAUTION: The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

- **Package Contents**
- PXIe-9852 high-speed digitizer
- ADLINK All-in-one compact disc
- PXIe-9852 Quick Start Guide

If any of these items are missing or damaged, contact the dealer

WARNING: Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/vendor immediately for assistance and obtain authorization before returning any product.

2.2 Installing the Module

1. Turn off the PXIe system/chassis and connect the power cable from the power source.

NOTE: Connection of the power cable provides grounding to prevent hazardous ESD (electrostatic discharge).

2. Align the module's edge with the module guide in the PXIe chassis.
3. Slide the module into the chassis until resistance is felt from the PXIe connector.
4. Push the ejector latch upwards and fully insert the module into the chassis.

5. Once the module is fully seated, a “click” can be heard from the ejector latch.
6. Tighten the screw on the front panel.
7. Power up the PXIe system/chassis.

NOTE: The red ejector latch lock must be depressed before the module can be uninstsalled.

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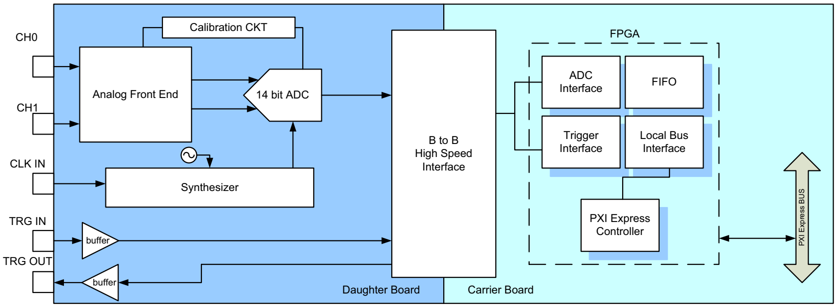
3 Operations

This chapter contains information regarding analog input, triggering and timing for the PXIe-9852.

3.1 Functional Block Diagram



3.2 Analog Input Channel

3.2.1 Analog Input Front-End Configuration

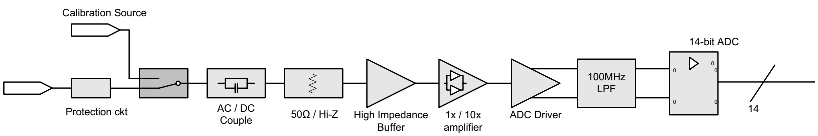


Figure 3-1: Analog Input Architecture of the PXIe-9852

Input Configuration

The input channel terminates with equivalent 50Ω or 1 MΩ input impedance (selected by software). The 14-bit ADC provides not only accurate DC performance but also high signal-to-noise ratio, and high spurious-free dynamic range in AC performance. The ADC transfers data to system memory via the high speed PCI Express Gen2 X 4 interface.

For auto-calibration, internal calibration provides stable and accurate reference voltage to the AI.

3.2.2 Input Range and Data Format

Data format of the PXIe-9852 is 2's complement. The ADC data of PXIe-9852 is on the 14 MSB of the 16-bit A/D data. The 2 LSB of the 16-bit A/D data should be truncated by software. A/D data structure is as follows.

D15	D14	D13	D12	....	D3	D2	D1	D0
D15 ~ D2 bits represent the data from ADC (2's complement) D1, D0 bits are always 0.								

Table 3-1: Input Range and Data Format

Description	Full scale range	Least significant bit	FSR-1LSB	-FSR
Bipolar Analog Input	±10V	1.22mV	9.99878V	-10.000V
	±2V	0.244mV	1.99976V	-2V
	±0.2V	24.4uV	0.199976V	-0.2V
Digital Code	N/A	N/A	7FFC	8000

Table 3-2: Input Range FSR and –FSR Values

Description		Midscale +1LSB	Midscale	Midscale -1LSB
Bipolar Analog Input	±10V	1.22mV	0V	-1.22mV
	±2V	0.244mV	0V	-0.244mV
	±0.2V	24.4V	0V	-24.4μV
Digital Code		0004	0000	FFFC

Table 3-3: Input Range Midscale Values

3.2.3 DMA Data Transfer

The PXIe-9852, a PCIe Gen 2 X 4 device, is equipped with a 200MS/s high sampling rate ADC, generating a 800 MByte/second rate.

To provide efficient data transfer, a PCI bus-mastering DMA is essential for continuous data streaming, as it helps to achieve full potential PCI Express bus bandwidth. The bus-mastering controller releases the burden on the host CPU since data is directly transferred to the host memory without intervention. Once analog input operation begins, the DMA returns control of the program. During DMA transfer, the hardware temporarily stores acquired data in the onboard AD Data FIFO, and then transfers the data to a user-defined DMA buffer in the computer.

Using a high-level programming library for high speed DMA data acquisition, the sampling period and the number of conversions needs simply to be assigned into specified counters. After the AD trigger condition is met, the data will be transferred to the system memory by the bus-mastering DMA.

In a multi-user or multi-tasking OS, such as Microsoft Windows, Linux, or other, it is difficult to allocate a large continuous memory block. Therefore, the bus controller provides DMA transfer with scatter-gather function to link non-contiguous memory blocks into a linked list so users can transfer large amounts of data without being limited by memory limitations. In non-scatter-gather mode, the maximum DMA data transfer size is 2M double words (8 M bytes); in scatter-gather mode, there is no limitation on DMA data transfer size except the physical storage capacity of the system.

Users can also link descriptor nodes circularly to achieve a multi-buffered DMA. Figure 3-2 illustrates a linked list comprising three DMA descriptors. Each descriptor contains a PCI address, PCI dual address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual address support 64-bit addresses which can be mapped into more than 4 GB of address space.

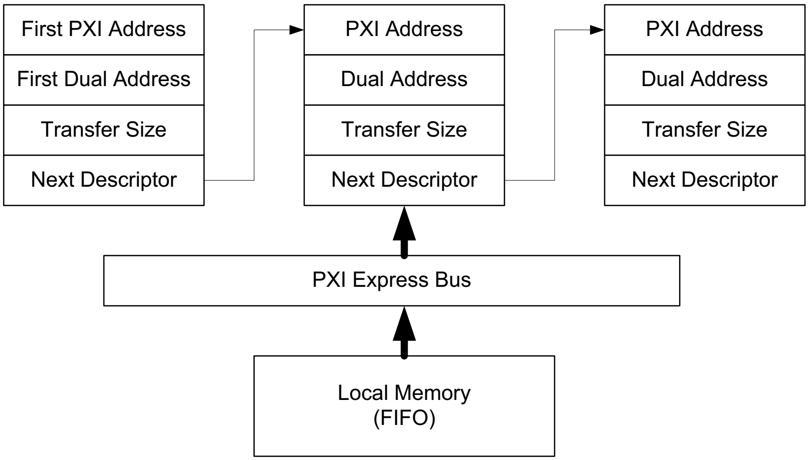


Figure 3-2: Linked List of PCI Address DMA Descriptors

3.3 Trigger Source and Trigger Modes

This section details PXIe-9852 triggering operations.

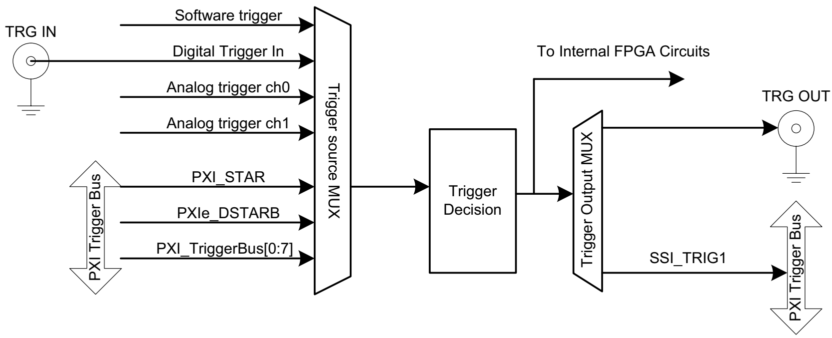


Figure 3-3: Trigger Architecture of the PXIe-9852

The PXIe-9852 requires a trigger to implement acquisition of data. Configuration of triggers requires identification of trigger source. The PXIe-9852 supports internal software trigger, external digital trigger, and analog trigger.

3.3.1 Software Trigger

The software trigger, generated by software command, is asserted immediately following execution of specified function calls to begin the operation.

3.3.2 External Digital Trigger

An external digital trigger is generated when a TTL rising edge or falling edge is detected at the SMA connector TRG IN on the front panel. As shown, trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL compatible, and the minimum pulse width 20 ns.

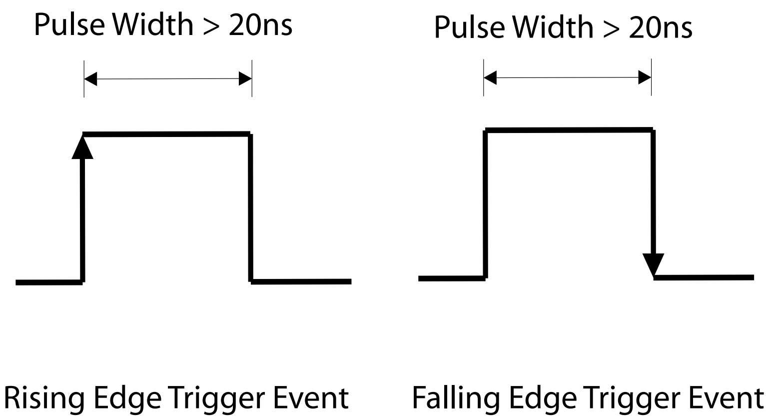


Figure 3-4: External Digital Trigger

3.3.3 PXI STAR Trigger

When PXI STAR is selected as the trigger source, the PXIe-9852 accepts a TTL-compatible digital signal as a trigger signal.

Triggering occurs when a rising edge or falling edge is detected at PXI STAR, with trigger polarity configurable by software. The minimum pulse width requirement of this digital trigger signal is 20 ns.

3.3.4 PXIe_DSTARB Trigger

The PXIe_DSTARB signal, a differential signal transmitted via the PXI Express Chassis backplane, distributes high-speed, high-quality trigger signals. When PXIe_DSTARB is selected as the trigger source, the PXIe-9852 accepts a fast-switching LVDS digital signal as a trigger signal. Triggering occurs when a rising edge or falling edge is detected at PXIe_DSTARB, with trigger polarity configurable by software, with minimum pulse width requirement of 20 ns.

3.3.5 PXI Trigger Bus

The PXIe-9852 utilizes PXI Trigger Bus Numbers 0 through 7 to act as a System Synchronization Interface (SSI). With the interconnected bus provided by PXI Trigger Bus, multiple modules are easily synched. When configured as input, the PXIe-9852 serves as a slave module and can accept trigger signals from one of buses 0 through 7. When configured as output, the PXIe-9852 serves as a master module and can output trigger signals to the PXI Trigger Bus Numbers 0 through 7.

3.3.6 Analog Trigger

An analog trigger is generated when AI input signal level is detected at the SMA connector CH0, CH1 (selected by software). The trigger level is also selected by software.

3.3.7 Trigger Export

When acquisition is initiated, a pulse synchronized with the Timebase clock asserts and is output through trigger output, at a pulse width programmable from 50ns to 10μs via software.

3.4 Trigger Modes

Trigger modes applied to trigger sources initiate different data acquisition timings when a trigger event occurs. The following trigger mode descriptions are applied to analog input function.

3.4.1 Post Trigger Mode

Post-trigger acquisition is applicable when data is to be collected after the trigger event, as shown. When the operation starts, PXIe-9852 waits for a trigger event. Once the trigger signal is received, acquisition begins. Data is generated from ADC and transferred to system memory continuously. The acquisition stops once the total data amount reaches a predefined value.

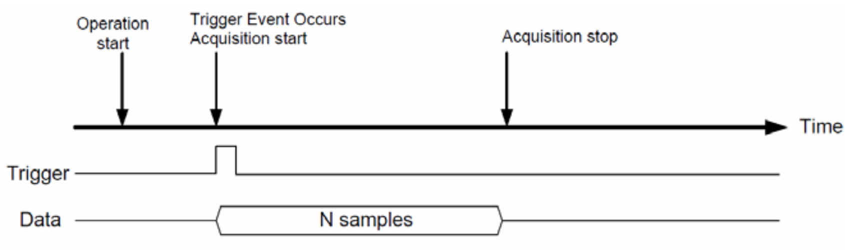


Figure 3-5: Post-Trigger Acquisition

3.4.2 Delayed Trigger Mode

Delayed-trigger acquisition is utilized to postpone data collection after the trigger event, as shown. When PXIe-9852 receives a trigger event, a time delay is implemented before commencing acquisition. The delay is specified by a 16-bit counter value such that a maximum thereof is the period of TIMEBASE X (2^{16}), and the minimum is the Timebase period.

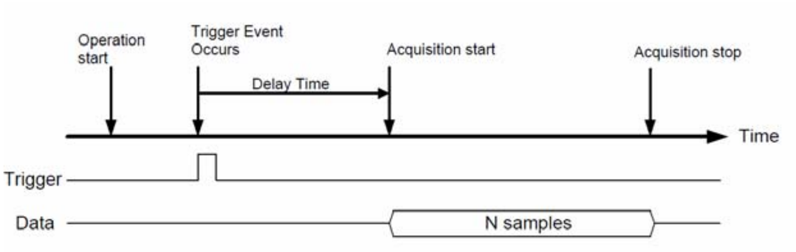


Figure 3-6: Delayed Trigger Mode Acquisition

3.4.3 Pre-Trigger Mode

Collects data before the trigger event, starting once specified function calls are executed to begin the pre-trigger operation, and stopping when the trigger event occurs. If the trigger event occurs after the specified amount of data has been acquired, the system stores only data preceding the trigger event by a specified amount, as follows.

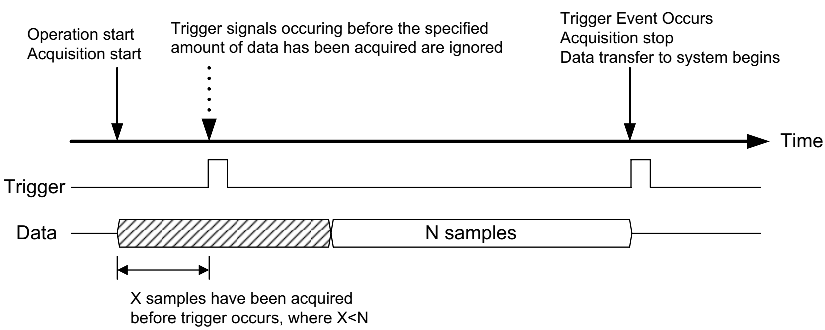


Figure 3-7: Pre-Trigger Mode Acquisition

3.4.4 Middle Trigger Mode

Collects data before and after the trigger event, with the amount to be collected set individually (M and N samples), as follows

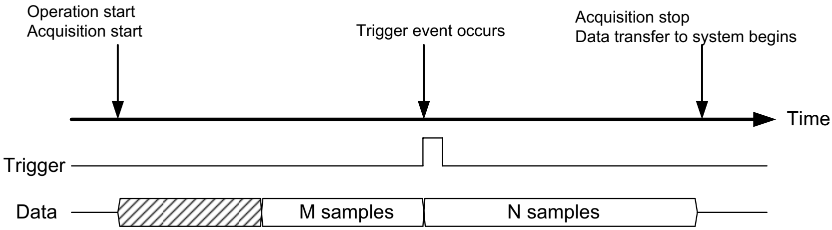


Figure 3-8: Middle Trigger Mode Acquisition

3.4.5 Acquisition with Re-Triggering

A digitizer acquires a trace of N samples/channel for a single acquisition. Re-Trigger mode can also be set to automatically acquire R traces, containing N*R samples/channel of data, without additional software intervention.

The Re-Trigger setting can be used for Post-Trigger and Delayed-Trigger modes, with different limitations on the spacing between trigger events in each mode. Trigger events arriving too close to the previous instance will be ignored by the digitizer.

- In Post-Trigger mode, the minimum spacing between trigger events is N+8
- In Delayed-Trigger mode, the minimum spacing between trigger events is (N+D)+8, where D is the number of the delayed setting

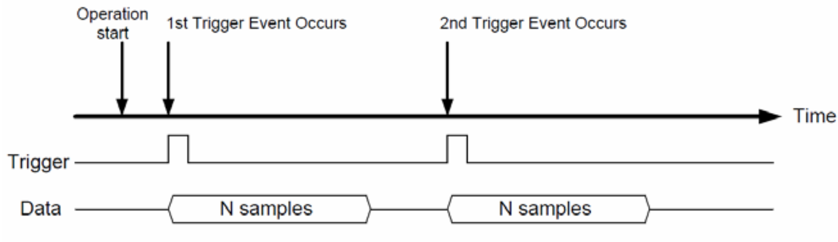


Figure 3-9: Re-Trigger Mode Acquisition

3.4.6 Data Average Mode (Post-Trigger and Delayed-Trigger only)

In normal post-trigger mode acquisition, N samples/channel data are generated for a single trigger event. In Re-trigger mode (See "Acquisition with Re-Triggering" on page 23.), a total of N * R samples/channel data is generated for R trigger events, that is, R traces (A trace contains N samples/channel). In Data Average Mode, only N samples/channel data are generated for R trigger events. The single trace data (N samples/channel) is the average of the R traces sample by sample.

The output data format is 16-bit or 32-bit signed integer, software selectable. When higher measurement accuracy is desired, data average mode with 32 bit data output can improve the resolution. According to oversampling practice, the retrigger times R required to get n bits of additional resolution is R = 4^n. Please note that in order for data average mode to work properly, components of signal of interest, such as period and magnitude, should be consistent during conversion.

3.5 Timebase

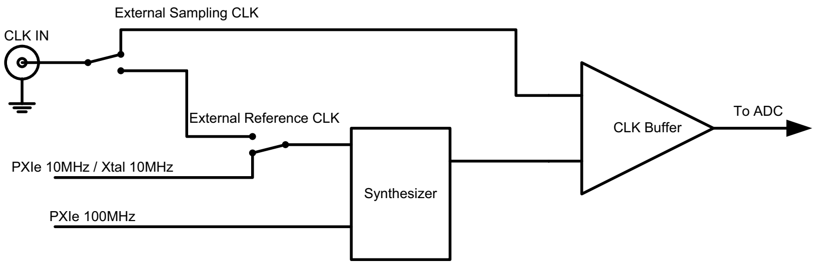


Figure 3-10: PXIe-9852 Clock Architecture

3.5.1 Internal Reference Clock

The PXIe-9852 internal 10MHz Crystal oscillator acts as reference clock, generating, after synthesis, precisely 200MHz clock for ADC.

3.5.2 External Reference Clock

The PXIe-9852 can choose an external clock source for use as a reference clock. When an external clock reference is selected, the synthesizer input will switch to the clock source at SMA connector CLK IN, and generate precisely 200MHz clock for ADC. The frequency of clock source is restricted to 10MHz.

3.5.3 External Sampling Clock

The PXIe-9852 can further choose an external clock source as ADC sampling clock. When an external sampling clock is selected, the ADC sampling frequency switches to the clock source at SMA Connector CLK IN, and clock source frequency is available from 40MHz to 200MHz.

3.5.4 PXI_CLK10 Clock

The PXIe-9852 can receive the timebase from the PXI_CLK10 Clock, the signal of which originates at the PXI Express chassis backplane, matched in propagation delay within 1 ns.

3.5.5 PXI_CLK100 Clock

The PXIe-9852 can receive the timebase from the PXI_CLK100 Clock, the signal of which originates at the PXI Express chassis backplane, matched in propagation delay within 200 ps.

3.6 ADC Timing Control

3.6.1 Timebase Architecture

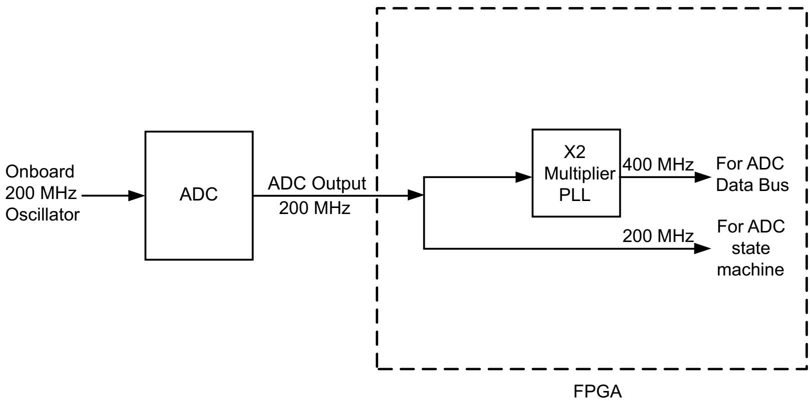


Figure 3-11: PXIe-9852 Timebase Architecture

3.6.2 Basic Acquisition Timing

The PXIe-9852 commences acquisition upon receipt of a trigger event originating with software command, external digital trigger, or the PXIe Trigger Bus. The Timebase is a clock provided to the ADC and acquisition engine for essential timing. The Timebase is from an onboard synthesizer. To achieve different sampling rates, a scan interval counter is used.

Using the post-trigger mode as an example, as shown, when a trigger is accepted by the digitizer, the acquisition engine commences acquisition of data from ADC, and stores the sampled data to the onboard FIFO. When FIFO is not empty, data will be transferred to system memory immediately through the DMA engine. The sampled data is generated continuously at the rising edge of Timebase according to the scan interval counter setting. When sampled data reaches a specified value, in this example 256, acquisition ends.

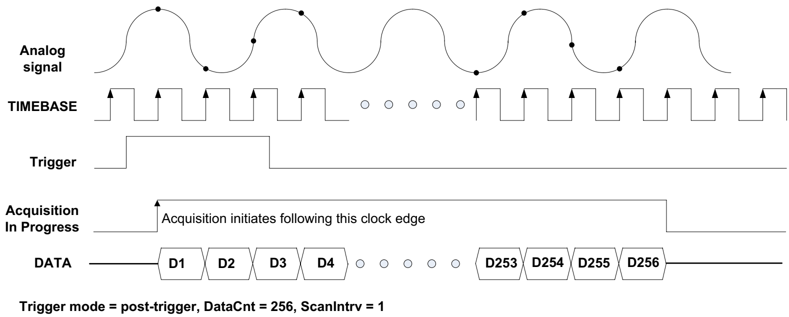


Figure 3-12: Basic Digitizer Acquisition Timing

To achieve sampling rates other than 200MS/s, a number for scan interval counter needs only be specified. For example, if the scan interval counter is set as 2, the equivalent sampling rate is 200MS/s / 2 = 100MS/s. If as 3, the equivalent sampling rate is 200MS/s / 3 = 66.66MS/s, and vice versa. The scan interval counter is 16 bits in width, therefore the lowest sampling rate is 3.051KS/s (200MS/s / 65535).

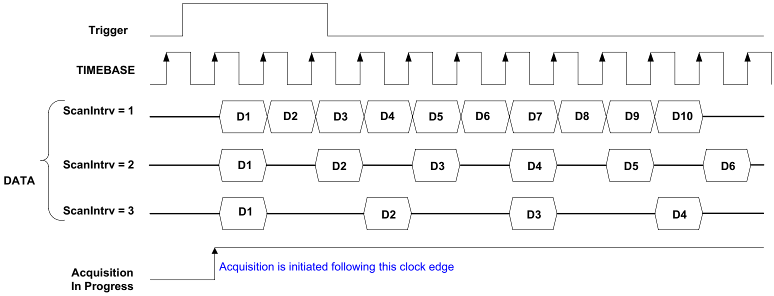


Figure 3-13: Varying Sampling Rates by Adjusting Scan Interval Counter

Counter Name	Length	Valid Value	Description
ScanIntrv	16-bit	1-65535	Timebase divider to achieve equivalent sampling rate of the digitizer, where Sampling rate = Timebase / ScanIntrv
DataCnt	28-bit	1-268435452	Specifies the amount of data to be acquired: ▶ 1 - 268435452 for pre-trig or mid-trig mode operation ▶ 1 - 268435452 for Data Average mode for 1 channel ▶ 1 - 134217724 for Data Average mode for 2 channel
trigDelayTicks	16-bit	1 -65535	Indicates time between a trigger event and commencement of acquisition. The unit of a delay count is the period of the Timebase.

Counter Name	Length	Valid Value	Description
ReTrgCnt	31-bit	1-2147483647	Enables re-trigger to accept multiple triggers. ▶ 1 - 2147483647 for normal operation ▶ 1 - 65535 for Data Average mode See Acquisition with Re-Triggering

Table 3-4: Counter Parameters and Description

3.7 Synchronizing Multiple Modules

The SSI (System Synchronization Interface) of the PXIe-9852 is achieved by a trigger signal, pre_data_ready signal(s) and a reference clock, all transmitted through PXI_BUS ports to enable multiple module synchronization. When synchronizing multiple devices, a PXIe-9852 can be configured as a master or a slave, wherein the system accommodates multiple slave devices but only a single master device. For better synchronization between multiple devices, all connected PXIe-9852s should refer to the same time base. The time base can be PXI_CLK 10, PXIe_CLK 100, or an external clock through the front panel.

When operating in post-trig or delay-trig mode, the only trigger signal transmitted through PXI BUS is SSI_TRIG1, used to initiate acquisition of all devices. A master device should set one PXI_BUS pin in output direction. The trigger signal will be sent out through this pin to other slave devices on PXI_BUS. All slave devices should set the trigger signal from the corresponding PXI_BUS pin so that all devices on PXI_BUS are triggered simultaneously.

When any device on PXI_BUS is required to operate in pre-trig or mid-trig mode, the master device must be set correspondingly. The trigger modes of other slave devices are not limited. A slave device in pre-trig/mid-trig mode transmits a pre_data_ready signal to inform the master device that it is ready to accept trigger signals (for more details of pre-trig and mid-trig status, please see "Pre-

Trigger Mode” on page 22. and “Middle Trigger Mode” on page 23.). This slave device should set one PXI_BUS pin, not used to transmit and receive SSI_TRIG1, to output to transmit its pre_data_ready signal to master device. If any other slave device is in pre-trig/mid-trig mode, it should set another PXI_BUS pin to send its pre_data_ready signal. In this scenario, a single line on PXI_BUS is used to transmit trigger signals from master to slave, while other specified lines are used to transmit pre_data_ready signals from slave devices in pre-trig/mid-trig mode to a master device. From the master device, one pin is assigned as output to transmit trigger signal. The trigger signal won’t be sent out until all slaves’ pre_data_ready is received by the master device.

Appendix A Calibration

This chapter introduces the calibration process to minimize analog input measurement errors.

A.1 Calibration Constant

The PXIe-9852 is factory calibrated before shipment, with associated calibration constants written to the onboard EEPROM. At system boot, the PXIe-9852 driver loads these calibration constants, such that analog input path errors are minimized. ADLINK provides a software API for calibrating the PXIe-9852.

The onboard EEPROM provides two banks for calibration constant storage. Bank 0, the default bank, records the factory calibrated constants, providing written protection preventing erroneous auto-calibration. Bank 1 is user-defined space, provided for storage of self-calibration constants. Upon execution of auto-calibration, the calibration constants are recorded to Bank 1.

When PXIe-9852 boots, the driver accesses the calibration constants and is automatically set to hardware. In the absence of user assignment, the driver loads constants stored in bank 0. If constants from Bank 1 are to be loaded, the preferred bank can be designated as boot bank by software. Following re-assignment of the bank, the driver will load the desired constants on system reboot. This setting is recorded to EEPROM and is retained until reconfiguration.

A.2 Auto-Calibration

Because errors in measurement and outputs will vary with time and temperature, re-calibration is recommended when the module is installed. Auto-calibration can measure and minimize errors without external signal connections, reference voltages, or measurement devices.

The PXIe-9852 has an on-board calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured on the production line and recorded in the on-board EEPROM.

Before initializing auto-calibration, it is recommended to warm up the PXIe-9852 for at least 20 minutes and remove connected cables.

NOTE: It is not necessary to manually factor delay into applications, as the PXIe-9852 driver automatically adds the compensation time.

Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

WARNING: Risk of explosion if battery is replaced with an incorrect type; please dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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